Abstract

The thesis dealt with clock and data recovery (CDR) circuit, using linear phase detector (PD) for high-speed wireline data communication receiver.

In the proposed architecture, a linear PD has been implemented for CDR with proportional pulse width of 2 *UI* at nominal phase position between data and clock. The PD architecture developed in this work, achieves highest proportional pulse width at nominal phase position, compared to conventional architectures, using quarter rate four phase clock.

Furthermore, a tunable current mode logic (CML) delay cell, based on hysteresis in switching threshold principle, has been introduced. A wide and linearly tunable ring-VCO using two stages of proposed delay cells has been realized to obtain clock source for the CDR.

A test chip has been realized in 65 nm CMOS process. For validation of the proposed design, on chip 12.5 Gb/s PRBS-15 serial data is generated from four parallel random data stream. This data is then fed to the dual loop CDR. A 3.125 GHz clock from ring-VCO has been recovered and phase aligned 1:4 demultiplxed data at a rate of 3.125 Gb/s are generated. RMS and peak-peak jitter of 2.2 ps and 17.9 are observed in the recovered 1/4 rate clock. Opening of recovered data eye suggests Bit Error Rate (BER) is less than 10^{-12} with PRBS-15 sequence. The proposed PD achieves 18 % increment of linear phase detection range with respect to bit *UI* and 100 % improvement in phase error gain compare to conventional works Overall CDR achieves power efficiency of 7.1 Gb/s/mW at 12.5 Gb/s data rate with core supply of 1.2V, consuming core silicon area of 0.236 mm^2.

Both delay cell and ring VCO are thoroughly characterized through simulation and measurement. VCO covers a coarse frequency tuning range around 2 to 9 GHz. The scheme also incorporates a fine frequency tuning range with 68% linearity with respect to input control voltage. The measurement shows proposed VCO achieves approximately 9.5 GHz/V and an average of 150 MHz/V coarse and fine VCO transfer gain respectively. Four phase VCO consumes 6.4 mW of power including buffers, with core supply of 1.2V.