ABSTRACT

Key words : *Polysilicon, LPCVD, ion beam sputtering, grain, grain-boundary, annealing, diffusion, microstructure, conductivity, Hall mobility, polyresistor, TCR, aspect ratio, grain-boundary barrier, scattering potential, trapped charge, thermionic emission, tunneling, field emission, large-bias conduction, electrical trimming, Joule heating, passivation, recrystallisation, threshold current density, fuse-link, fusing delay, minimum power density, second breakdown.*

The present thesis deals with the study of the large-bias conduction and some high-current-induced effects in ion-beam-sputtered polycrystalline silicon films for microelectronic applications.

In order to understand the physical mechanism of electrical conduction in polysilicon films and to develop a large-bias conduction model, an exhaustive review of the different electrical conduction models of polysilicon films has been made (Chapter-2). It outlines the chronological development of models based on various concepts, such as dopant segregation, carrier trapping, thermionic emission and tunneling, drift-diffusion, etc. and makes a comparative study of the different classes of models.

The ion beam sputtering technique has been investigated to deposit polysilicon films suitable for microelectronic applications (Chapter-3). The microstructural and electrical properties of as-deposited films as well as films post-processed by annealing and by thermal-diffusion of impurities have been investigated. Films of average grain size 400 Å - 800 Å and principal growth textures along $\langle 420 \rangle$, $\langle 200 \rangle$ and $\langle 331 \rangle$ have been obtained. The average Hall mobility of phosphorus doped films varied from 3 to 87 cm^2/V-sec for carrier concentrations in the range of 5×10^{18} cm^{-3} to 10^{21} cm^{-3}. Oxide isolated monolithic resistors of different aspect ratios have been fabricated by the photolithographic patterning of doped polysilicon films.

A large-bias conduction model has been developed by extending the emission-based carrier trapping models [5,7] valid for small-signal, small-bias conditions (Chapter-4). The large-bias effects which have been incorporated are the asymmetry of space charge potential barrier around the grain bound-

ary layers, finite potential drop in the grains and the avalanche multiplication of carriers in the grain boundaries. The model has been validated with the experimental data on I-V characteristics of ion-beam-sputtered polyresistors measured using a single-pulse measurement technique to avoid any morphological change of grain boundaries due to localised Joule heating. The grain-boundary related model parameters were extracted from experimental data on the temperature dependence of small-bias resistivity around the room temperature.

A detailed experimental study has been carried out on the high-current pulse trimming of ion-beam-sputtered polysilicon resistors doped heavily with phosphorus (Chapter-5). The duty cycle of the pulses was kept sufficiently low so that the average temperature could not rise appreciably. The resistance of the polyresistor was found to decrease steadily with increasing current as the peak current density exceeded $\sim 5\times10^5$ A/cm^2. The maximum trimming range of a 95 μm long, 4.9 μm wide, 0.5 μm thick polyresistor of initial resistance 2600 ohm has been found to be -27 %. The I-V characteristics were also recorded during the trimming process. The trimming characteristics and the I-V characteristics have been fitted with theoretical models by adjusting the grain-boundary-related parameters appropriately. The nature of variation of these parameters with the peak current density of pulses has helped in understanding the physical processes responsible for trimming. The transient heating of highly resistive, ultra-thin grain-boundary layers due to high-current pulse stressing is predicted to cause passivation and zone melting-cum-recrystallisation of GB layers, resulting in the decrease of resistance.

A study of the current and voltage transients of heavily doped polysilicon fuse-links has also been undertaken (Chapter-6). The power-delay characteristics, the dynamic I-V characteristics and the variation of resistance with time upto the fuse-off instant have been investigated. Typical fusing delays of 5 - 60 μsec for the input power of 2.3 W - 1.7 W were obtained for fuse-link of resistance 350 $\pm$ 15 ohm. The formation of a current filament during the fusing operation has been revealed through microscopic observations of fused resistors. The results have been qualitatively discussed in the light of a second breakdown process that is believed to occur during the fusing transition.