Abstract

Very exciting and promising results from the group-IV alloy layers have led to the belief that silicon-germanium (SiGe) based devices will open up an entirely new dimension in VLSI/ULSI Si technology. Strained $Si_{1-x}Ge_x$ and strain compensated $Si_{1-x-y}Ge_xC_y$ offer many desirable electronic and optical properties due to favorable band alignment and strain-induced modification of band structure, effective mass and optical transitions. Growth of gate quality ultrathin oxide/stacked oxynitride films is a key technology issue in device scaling efforts since they form the 'heart' of n- and p-channel MOSFETs in CMOS technology and largely determine the transistor's performance. Low-temperature growth of ultrathin dielectrics on SiGe/SiGeC layers are attractive for device applications since strained SiGe and partially strain compensated SiGeC layers (typically grown at ~550°C) are metastable in nature.

The present research study is concerned with the investigation on $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ heterolayers for high performance p-MOSFET applications. The following studies have been carried out in detail:

- Heterostructures $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ layers have been grown using GSMBE and UHVCVD. Microstructural characterization of the films have been performed using RBS, SIMS, HRXRD and AFM techniques.
- Hole confinement in SiGe/SiGeC well has been used to determine the valence band offset and threshold voltages at surface and buried channels of a MOS capacitor. Minority carrier generation lifetime of binary and ternary alloy layers has been measured from transient response of a MOS capacitor.
- Growth of ultrathin oxide (<100 Å) on SiGe/SiGeC layers has been performed using microwave plasma at a low temperature.
- Stacked oxynitride films (viz., NH_3/NO, $O_2/NO/O_2$, $NO/O_2/NO$ and $O_2/NH_3/NO$) grown using plasma process exhibit improved electrical, interfacial, charge trapping and reliability properties.
- Design and simulation of heterostructure SiGe-channel p-MOSFETs on modulation-doped layer and SIMOX substrates have been carried out using 1-D Poisson solver, analytical model and Silvaco-ATLAS device simulation tool.