Abstract

With the switching abilities of present day semiconductor devices (such as the MOSFETs/IGBTs) and the processing speeds of present day digital controllers (such as microprocessors/microcontrollers/DSPs/FPGAs), switching frequencies of several kHz are generally applied for motor drives, especially in the lower power applications with ratings up to tens of kilowatts. Good bandwidth for torque current control can be achieved in these drives. Also, even if the speed of the drive extends to voltage-limited field weakening region, the inverter can still be operated in PWM mode provided that the controlled dc-link voltage is derived from the unity power factor boost converter.Same is not true for medium voltage traction drives using semiconductor switches with higher voltage blocking capacity. In the medium voltage level, the semiconductors (IGBTs/GTOs) switch at a lower frequency (200Hz-500Hz) to restrictthe switching losses within reasonable bounds. Due to the lower switching frequency of the traction converters, the harmonic profile of the inverter pole voltage deteriorates. Hence, it is necessary to maintain synchronisation, three phase symmetry, half wave symmetry and quarter wave symmetry of the inverter pole voltage waveforms. Also, the traction drives need to operate at the deep field weakening region (2 to 3 times the base speed) to optimize the utilization of the motor ratings.

This work proposes a carrier based synchronised sinusoidal PWM technique along with a compatible over modulation algorithm for a two-level inverter to operate the semiconductor switches at a lower frequency. The proposed synchronous PWM technique maintains synchronisation in both steady and dynamic conditions as the synchronous carriers are generated from the instantaneous voltage references. The concept of synchronous PWM technique is also extended to the multilevel inverter topologies i.e. for LSPWM and PSPWM techniques. This work analytically explains the conditions to maintain synchronisation, three phase symmetry, half-wave symmetry and quarter wave symmetry of the pole voltage waveforms of a cascaded H-Bridge multilevel inverter (CHBMLI). A field weakening control scheme is also developed, which maintains current control for an induction motor drive even when the two-level inverter enters the Six-Step Mode of operation. The PWM techniques and the field weakening control scheme are verified experimentally with the help of a squirrel cage induction motor drive supplied from either a two-level inverter or a five-level CHBMLI laboratory prototype, and the experimental results are presented to validate their usefulness.