Abstract

The on-going demand of real-time video applications has put forward new challenges in the domain of video coding. One of them has been the efficient design of motion estimation (ME) unit that plays a significant role by exploiting and reducing the temporal redundancies that exist between consecutive frames in a sequence. The widely accepted Block Matching Algorithms (BMAs) provide simple and efficient ways to perform ME and have been adopted in current video coding standards. Therefore, the present work focuses on design and development of VLSI architectures for fast iterative and adaptive BMAs for motion estimation that are characterized by high speed and low area making them suitable for real-time video processing. Designs of low area architectures for popular Hexagonal Search and Adaptive Rood Pattern Search have been proposed. The proposed addressing mechanism and use of minimum number of processing elements contribute to the lowering of the on-chip area. Moreover, the current work has introduced efficient ME architectures for adaptive ME algorithms that involves reasonably limited on-chip area without compromising the real-time speed for transmitting High Definition videos. The proposed designs can tackle the adaptive nature of the algorithms and introduce efficient pattern generation scheme with an early SAD check technique to save the clock cycles. A new adaptive search algorithm for fast motion estimation and its dedicated VLSI architecture have also been developed. The competence of the algorithm lies in its efficiency to deal with large and small motion without going into any statistical computations and reduces the average number of search points per macroblock. Finally, the work presents an iterative and adaptive search strategy and a novel systolic array based architecture for the computation of fractional motion estimation, in addition to performing integer search. The work explores the inter level architecture that can adapt to multiple search strategies and perform a half-pixel resolution search. All the proposed architectures have been synthesized and analyzed for maximum operating frequencies, area utilization and power in FPGA platform.