Abstract

The Scalable video coding (SVC) extension of the traditional video coding method is able to very high throughput in data compression. However, it possesses considerable high complexity and low error resiliency to channel errors, which are not suitable for applications such as video surveillance, wireless camera sensor network, space exploration and sports broadcasting, where low complexity encoding is needed.

The present work has, therefore, focused on the development of a novel framework for Compressed Sensing based Scalable Video Coding (CS based SVC) and its VLSI implementation. The proposed framework achieves scalability through 3-Dimensional Discrete Wavelet Transform (3-D DWT) and better compression ratio by exploiting the inherent sparsity of the high-frequency wavelet sub-bands through CS. By using 3-D DWT and a proposed adaptive measurement scheme (AMS) at the encoder, one can succeed in improving the compression ratio and reducing the complexity of the decoder. The proposed CS based SVC uses only 12% of the total number of multipliers needed in a conventional CS-based video coding system. A codebook of Bernoulli matrices with different sizes corresponding to the predefined sparsity levels is maintained at both the encoder and the decoder. Based on the calculated ℓ_0-norm of the input vector, one of the sixteen possible Bernoulli matrices will be selected for calculating the CS measurement vector $\mathbf{y}$. The ℓ_0-norm (K) of the input vector is also transmitted with the CS measurement vector $\mathbf{y}$. Based on the K value, the corresponding Bernoulli matrix has been used in CS reconstruction algorithm to get back the high-frequency wavelet sub-bands at the decoder. At the decoder, a new Enhanced Approximate Message Passing (EAMP) algorithm has been proposed to reconstruct the wavelet coefficients and apply the inverse wavelet transform for restoring back the video frames.

An efficient hardware implementation for CS based SVC has also been presented in this thesis. The proposed hardware architecture consists of an encoder and a decoder. A high-speed memory efficient VLSI architecture for the encoder of a proposed CS based SVC has been implemented for space and low power video applications. The proposed encoder architecture consists of a high-speed 3-D DWT architecture and the efficient compressed sensing module (CS module). The 3-D DWT architecture, which has been designed with nine stage pipeline architecture, requires less memory and one can reap high throughput when compared with the best existing 3-D DWT architectures. The proposed architecture (which is based on DWT and CS) for an en-

coder is the first of its kind, and to the best of the authors' knowledge, no architecture is available in literature for comparison.

A novel architecture for the decoder of the proposed CS based SVC has been implemented using Enhanced Approximate Message Passing (EAMP) algorithm and the inverse 3-D DWT computation procedure. The EAMP algorithm shows better performance in terms of convergence rate and sparsity measurement trade-off while being compared to AMP, IST, and IHT. The execution time of the proposed design is reduced by maximizing parallelism with an appropriate level of unfolding. A high-speed memory efficient pipelined hardware architecture for 3-D inverse discrete wavelet transform is developed. Implementation results show that the proposed architecture benefits from features including reduced memory, low power consumption, low latency, and high throughput over several existing designs.

Index Terms : scalable video coding (SVC), compressed sensing (CS), 3-D discrete wavelet transform (3-D DWT), VLSI design, 3-D Inverse DWT (3-D IDWT), EAMP, AMP, IHT.