DESIGN METHODS TO ENHANCE STABILITY AND PERFORMANCE IN DIGITAL CURRENT MODE CONTROL IN DC-DC CONVERTERS

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by

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Abstract

Digital control of DC-DC converters has been growing at a rapid pace in the power electronics industries, because it offers various technical benefits. In fixed-frequency digital pulse-width-modulated (DPWM) DC-DC converters, current-mode control (CMC) offers improved bandwidth and stability margin over voltage-mode control (VMC); however, the former requires discretization of both the voltage and current information. While one sample per switching cycle is sufficient for the output voltage because of small ripple, the inductor current ripple is considerably large. Thus it is difficult to sample the fast-changing inductor current with the switching frequency beyond a few hundreds of kHz. Over the last decade, significant research efforts have been attempted to develop simple, cost-effective, and power-efficient digital CMC techniques.

This thesis considers existing digital CMC architectures and proposes a unified discrete-time framework for analyzing fast-scale instability under finite sampling. Approximate discrete-time models are derived and closed-form stability boundaries are obtained. The analysis shows that the use of finite current and/or voltage loop sampling in digital CMC often leads to fast-scale instability, considering the effective series resistance of the output capacitor. Further, design methods are proposed to enhance stability boundary with fast transient performance. The proposed discrete-time framework would be very helpful for power supply practitioners to understand underlying behavior under digital CMC and to devise stable digital control with fast response.

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Keywords:

Digital current mode control, buck and boost converters, continuous conduction mode, discrete-time modeling, finite sampling, sub-harmonic instability.