ABSTRACT

The present thesis embodies an in-depth study of 3-neighbourhood additive cellular automata (CA) and its application in testable VLSI circuit design. A brief survey on cellular automata and its various applications has been included. CA based multi-input signature analyzers have been analytically studied and their behaviours have been completely characterised. Reduction of BIST overheads through sharing of CA based BIST structures has been shown to improve test throughput significantly. A novel approach for synthesising easily testable finite state machines has been presented with CA as the basic building block. The proposed synthesis schemes show that incorporation of testability in the synthesis phase results in considerable reduction in test area overhead. The synthesised designs are shown to have better area delay performances compared to the existing methods. In the context of increased chip density, the need for an on-chip test controller is being stressed in recent times. Consequently, the problem of scheduling test vectors for testing different modules in a VLSI chip has attained a new dimension. A new test scheduling strategy has been worked out which suits very much with the changed situation. A CA based test controller design has been proposed.

KEYWORDS:

Design for Testability (DFT), Additive Cellular Automata (CA), Signature Analyzers, Aliasing Errors, Pseudo Random Testing, Built-In Self Test (BIST), Synthesis for Testability (SFT), State Assignment, Test Scheduling, Test Controller.