Abstract

This thesis involves design and development of new methods for the synthesis of PLA-based FSM's. Synthesis of a PLA-based FSM is usually performed in different phases. The logic synthesis phase involves optimization techniques like state assignment, factorization and decomposition of FSM's while topological design phase that follows logic design phase, involves optimization techniques like PLA folding. The methods developed in this thesis are primarily aimed at satisfying three major design goals 1) area 2) performance and 3) testability. State assignment has been identified as having the most critical influence on the generation of well optimized realizations with respect to each of these design goals. New state assignment techniques have been proposed that satisfy multiple design goals. This involves a state assignment technique targeting area and testability and a state assignment technique targeting area and performance. A new state assignment method has been developed that combines optimizations during logic design phase with those during topological design phase. A state assignment method targeting area minimization of a single FSM is not well suited for combined area minimization of cascaded FSM's. A new state assignment method applicable for cascaded FSM's has been presented. The capability of an optimization technique applied to an FSM is constrained heavily by the behaviour expressed in the State Transition Table (STT) of the FSM. A framework that modifies the STT of a given FSM while maintaining its functionality has been proposed and new optimization techniques for synthesis of PLA-based FSM's in such a framework have been designed. All the schemes have been implemented and tested.

Keywords: Programmable Logic Array (PLA), Finite State Machine (FSM), State Transition Table (STT), State Transition Graph (STG)