Chapter 1

Introduction

1.1 Background

1.1.1 Evolution of Microprocessors

Microprocessors are widely used in many applications such as computers, mobile phones, PDAs, digital cameras, etc.. These applications demand high performance microprocessor with small size. The historic trend of device scaling in the semiconductor device technology results in packing more number of transistors per unit area [1]. In particular, device scaling results in smaller die size for a given component

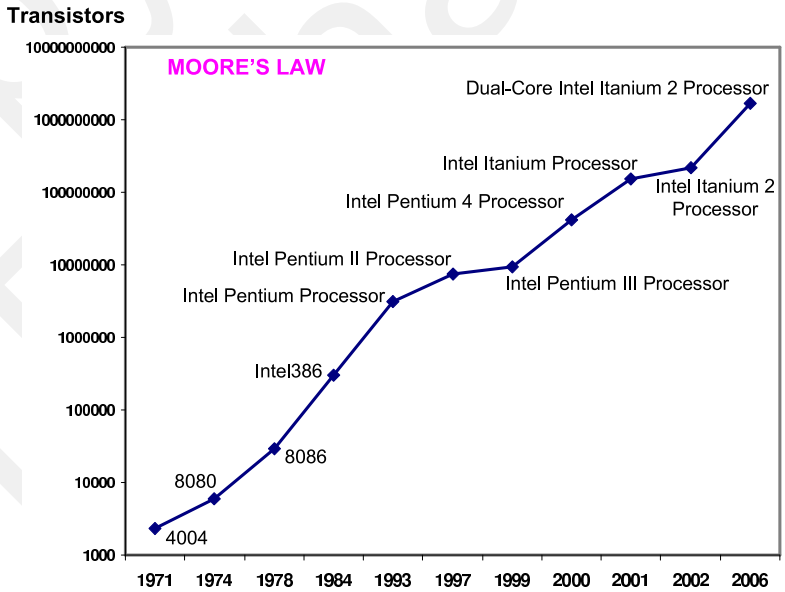

Figure 1.1: Number of transistors integrated on the CPU die for Intel processors [2]

complexity, higher speed of operation due to reduced logic circuit capacitance, lower voltage operation and high power density. Since the first microprocessor, Intel's 4004, was released in 1971 more and more transistors have been integrated in accordance with the Moore's law. Fig. 1.1 shows the historical data on the number of transistors integrated on an Intel central processing unit (CPU) die [2]. The Dual-Core Itanium 2 processor, which was released in 2006, has around 1.7 billion transistors which is about a million times more than the first 4004 microprocessor.

Today's microprocessors are operating at higher clock frequencies for faster computations which has increased their power consumption. The power consumption of a typical microprocessor [3] is given by

$$P_{\text{CPU}} = C\, V_{\text{cc}}^2\, f + P_{\text{leak}} \tag{1.1}$$

Where C denotes the equivalent power dissipation capacitance, V_{cc} is the supply voltage, f is the clock frequency of the microprocessor and P_{leak} is the power loss due to the leakage current*. Eqn. 1.1 illustrates that reduction in either supply voltage or clock frequency can minimize the power consumption of the microprocessors dramatically. Since device scaling permits lower voltage operation, it is clear that significant power reduction can be achieved by powering the microprocessor at low voltages. It is predicted that the future generation processors will run at very low voltage (0.8 V), and may consume currents in excess of 150 A (depending on the application) with slew-rate greater than 120 A/ns at the CPU die [4, 5]. Fig. 1.2(a) shows the historical data on the CPU core voltage and Fig. 1.2(b) shows the increasing trend of CPU current and slew-rate of Intel's microprocessors [4, 6, 7, 8, 9].

1.1.2 Power Distribution System in Mobile Computers

Before the introduction of the Pentium processors, the traditional centralized power supply (silver box) was sufficient to deliver all the necessary power to the Intel's processors. When the high performance Pentium processors emerged in the late 1990s, the centralized power system failed to meet the stringent power quality requirements. The power delivery path [10] from the 'silver box' to the processor is long enough to limit the power transfer speed. The impedance associated with the power delivery path severely affects the voltage regulation and efficiency of the power supply module.

*Leakage current occurs due to the finite resistance of a transistor in its OFF state between its high and low voltage sides and has recently become a major concern in nanometer transistors.

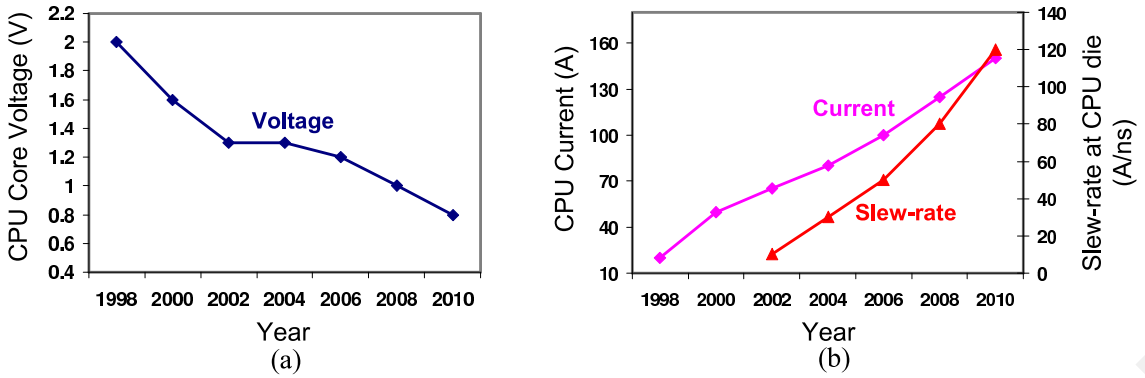

Figure 1.2: Historical data on (a) the CPU core voltage, (b) CPU current and slew-rate [Source: Intel]

Therefore, a dedicated power supply, the voltage regulator module (VRM) (also called the voltage regulator (VR) or power processing module (PPM)), is placed in close proximity to the processor in order to reduce the impedance associated with the power delivery path.

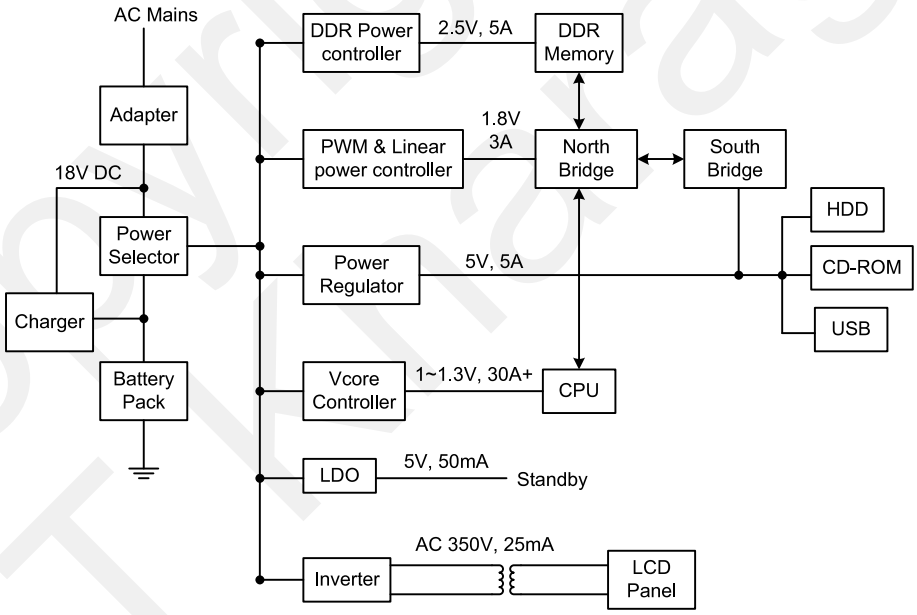

Figure 1.3: Typical block diagram of the power distribution system in a laptop computer [11]

Nowadays, laptop computers are gaining more of the market share compared to their desktop counterpart as they are light weight, easy to carry and comparable in cost and performance with the desktop computers. The typical block diagram of the

power distribution system in a laptop computer [11] is shown in Fig. 1.3. It has various types of power supply modules such as, AC adapter, DC/AC converter for LCD backlight, low-dropout (LDO) regulators, battery charger and DC/DC converters.

In general the source to power all the power supply modules in a laptop is either an AC adapter or a battery. The output voltage from the AC adapter is 19 V DC, whereas the battery voltage varies from 9∼16.8 V.

1.1.3 Intel Mobile Voltage Positioning Technology

In 1999, Intel introduced the first Intel mobile voltage positioning (I.M.V.P.) technology [12, 13] on Pentium-III processor to reduce the processor's power consumption. Traditional processor voltage regulators keep the processor voltage at a fixed level over all the processor activity states. The unique feature of the I.M.V.P. technology is that the processor voltage (V_{cc}) is dynamically adjusted based on the processor activity to reduce processor power consumption. I.M.V.P. voltage regulators set a lower allowable voltage during higher processor activity states (full-load).

Typical processor voltage regulators are designed to regulate V_{cc} as a static voltage over different static and dynamic load conditions. Fig. 1.4 illustrates a nominal V_{cc} setting centered between the processor voltage tolerance limits over a wide range of the processor current requirement. Specifically, three processor load conditions are indicated in Fig. 1.4. First one is the no-load condition when the processor is in the inactive state, second one is the typical load condition when the processor is actively running an application and the third is the thermal design power (TDP) load condition when the processor is being stressed. The I.M.V.P. technology takes advantage of the processor voltage tolerance limits to provide power reduction in both the typical and TDP load conditions. Fig. 1.5 shows an I.M.V.P. load line.

The following numerical example demonstrates the effectiveness of I.M.V.P. voltage regulator on reducing processor power over a traditional static voltage regulator. The processor power consumption is given roughly by

$$P_{\text{CPU}} = V_{cc}^2 X \tag{1.2}$$

where 'X' is a constant that depends on the clock frequency and the effective load capacitance.

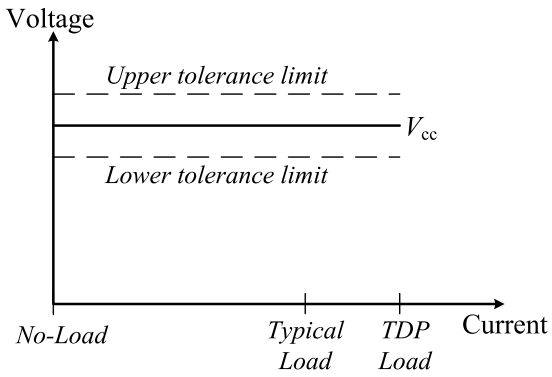

Figure 1.4: Static voltage regulation load line

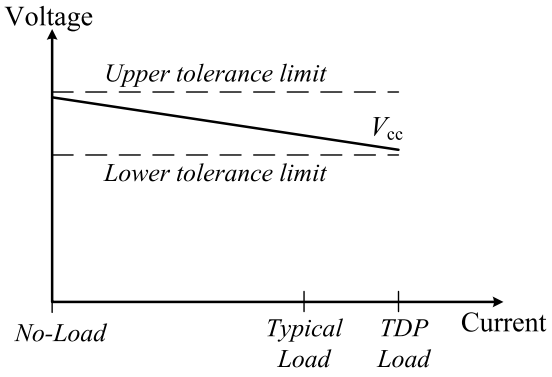

Figure 1.5: Intel mobile voltage positioning load line

The power consumption of the processor with the static processor voltage V_{STATIC} and with the I.M.V.P. processor voltage $V_{\text{I.M.V.P}}$ are given as

$$P_{\text{STATIC}} = V_{\text{STATIC}}^2 \, X \tag{1.3}$$

$$P_{\text{I.M.V.P}} = V_{\text{I.M.V.P}}^2 \, X \tag{1.4}$$

then the power consumption with I.M.V.P. feature is

$$P_{\text{I.M.V.P}} = P_{\text{STATIC}} \left(\frac{V_{\text{I.M.V.P}}}{V_{\text{STATIC}}} \right)^2 \tag{1.5}$$

Let us assume that the processor consumes 50 W of power with the static processor voltage of 1.5 V. Then with an I.M.V.P. voltage of 1.4 V the processor consumes only 43.55 W. The percentage of power saving using I.M.V.P. feature is

$$\frac{P_{\text{STATIC}} - P_{\text{I.M.V.P}}}{P_{\text{STATIC}}} = 12.88\% \tag{1.6}$$

Laptop thermal designers will benefit from this power reduction that the I.M.V.P. technology offers by allowing for thinner and lighter laptop cooling designs.

From Fig. 1.4 and Fig. 1.5, it is clear that the processor power consumption at light load is slightly higher with I.M.V.P. voltage regulator compared to a static voltage regulator. Setting the processor voltage just near to the lower tolerance limit under all load conditions can further reduce the processor power consumption. However this is not an optimal solution because the processor produces large transient currents when going from an inactive state to a full active state. These transients can cause the

processor voltage to violate the tolerance specifications of the processor leading to reliability and quality issues. Therefore, additional bulk capacitors will be required to meet the voltage tolerance specifications [14] which are more expensive and occupy significant motherboard space. The I.M.V.P. voltage regulator is designed to utilize the voltage tolerance window (upper tolerance limit−lower tolerance limit) during large load transients for capacitor reduction and to maintain lower allowable voltage at high load for power loss reduction.

With perfect I.M.V.P. implementation, the voltage regulator appears as an ideal voltage source in series with a constant resistance of value equal to the slope of the I.M.V.P load line. This raises the requirement of constant resistive output impedance for the VR. Thus the VR feedback control loop should be designed to achieve its closed loop output impedance to be equal to the slope of the I.M.V.P load line [15, 16, 17, 18]. References [19, 20] proposed VR design methodologies for selecting the output filter capacitors based on the constant output impedance requirement. Due to the benefits of power saving and passive filter capacitor reduction, the I.M.V.P. feature is widely incorporated in most of today's VR controller ICs [21, 22, 23, 24].

1.2 Voltage Regulators (VR)

1.2.1 Evolution of the VR

The evolution of VR began when the high performance Pentium processor was driven by a non-standard, less than 5 V power supply, instead of drawing its power from the 5 V plane on the system board [25]. At first, VRs drew power from the 5 V output of the SMPS box. As the power delivered through the VR increased dramatically, it no longer remained efficient to use the 5 V bus. Then, for desktop application, the VR input voltage was moved to the 12 V output of the SMPS box. For laptop application, the VR input voltage range covers the battery voltage range of 9∼16.8 V and the adaptor voltage of 19 V.

The microprocessors earlier to the Pentium processors were powered by the conventional buck converter from the 5 V output of the SMPS box. The conventional buck converter with its non-idealities is shown in Fig. 1.6. The fundamental limitations in achieving high efficiency can be understood from the following example.

Considering only the conduction losses, the efficiency is given by [26, 27],

$$\eta = \left(1 - \frac{V_{\mathrm{D}}(1-D)}{V_{\mathrm{o}}}\right) \left[\frac{1}{1 + \frac{R_{\mathrm{L}}}{R} + \frac{D.R_{\mathrm{S}}}{R}}\right] \tag{1.7}$$

where R_{S} is the ON-state resistance of the MOSFET 'S', V_{D} is ON-state voltage drop of the diode 'D_{fw}', R_{L} is the winding resistance of the filter inductor and D is the operating duty ratio.

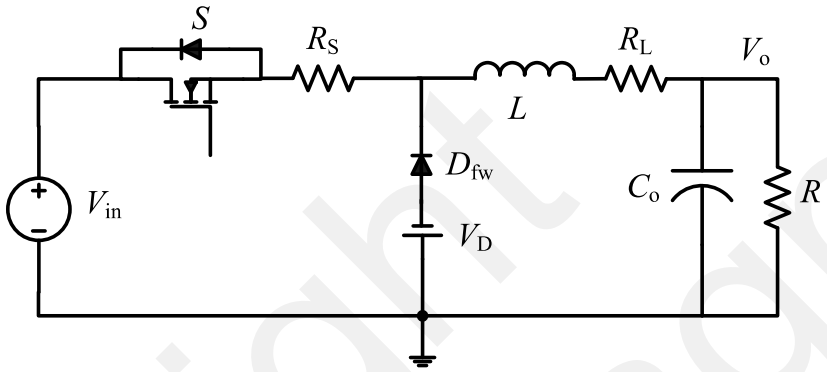

Figure 1.6: Conventional buck converter with circuit non-idealities

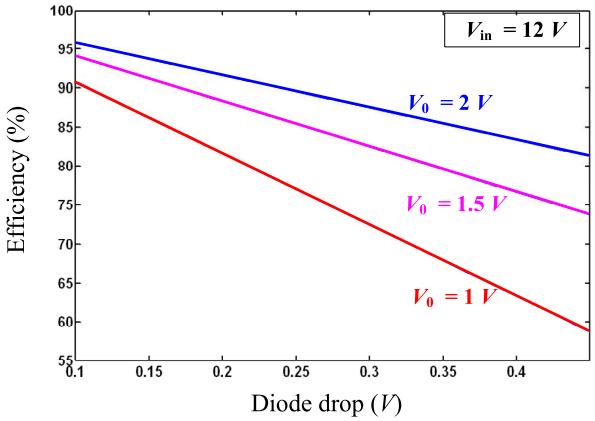

Figure 1.7: Effect of the diode voltage drop on efficiency

From Eqn. 1.7, it is clear that R_{S} and R_{L} should be small compared to the load resistance R. The voltage drop V_{D} across the freewheeling diode 'D_{fw}' significantly affects the efficiency especially at low output voltages. The variation of efficiency with the ON-state voltage drop of the diode is illustrated in Fig. 1.7. Hence for low voltage applications the freewheeling diode 'D_{fw}' in the conventional buck converter

has been replaced with low ON-resistance MOSFET to improve the efficiency. The modified circuit is popularly known as the synchronous buck converter (Fig. 1.8).

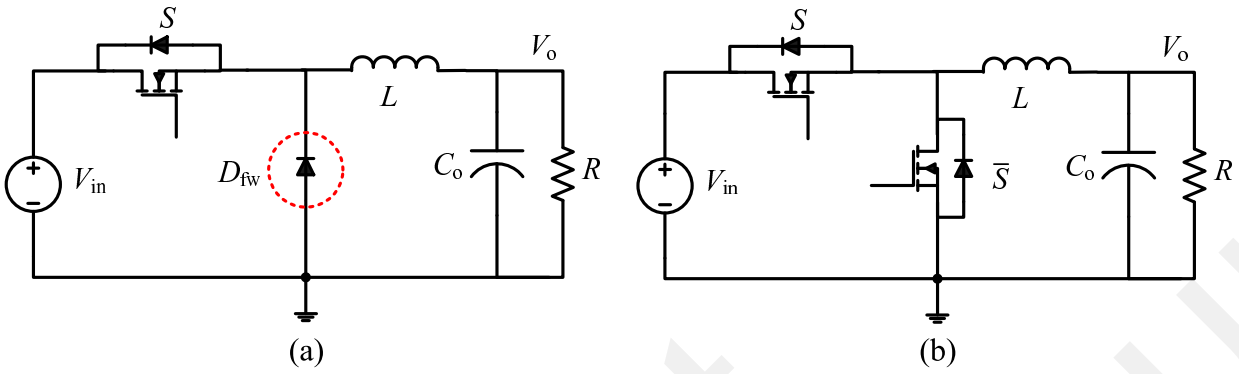

Figure 1.8: (a) Conventional buck converter (b) Synchronous buck converter

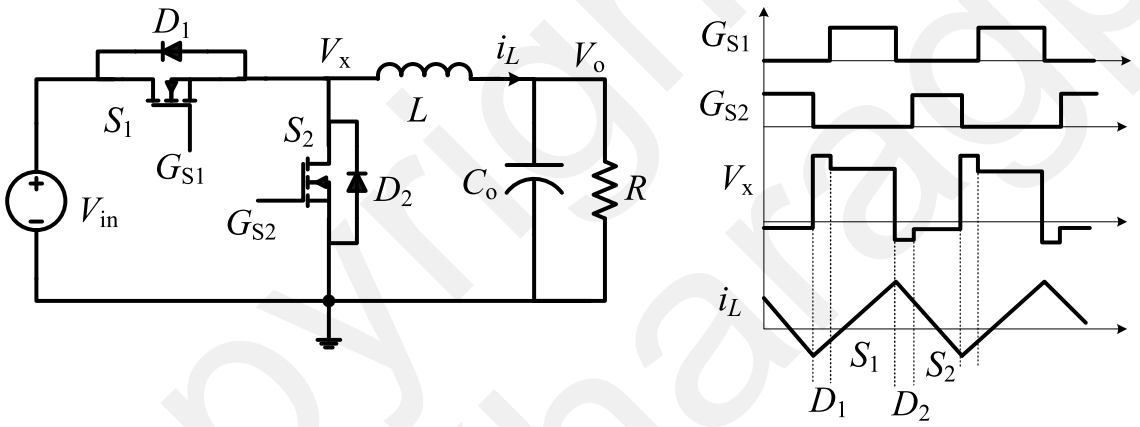

Figure 1.9: Quasi-square wave VR topology [28]

Voltage regulators have to supply large current at high slew-rate, when the microprocessor transits from the "sleep mode" to the "active mode" and vice-versa. The high efficiency requirement of the VR, restricts the operation of the synchronous buck converter to low frequency with a large output filter inductor, which limits the transient response of the output current. In order to meet the stringent microprocessor voltage tolerance requirements, large output filter capacitors are needed to reduce the voltage spikes during the transients [28, 29, 30]. To overcome the transient limitation, smaller filter inductance is desirable. Fig. 1.9 shows the quasi-square wave voltage regulator topology [28, 31], in which the inductor value is deliberately chosen 15 to 20 times smaller than that in a typical synchronous buck converter. The quasi-square wave (QSW) topology keeps the output filter inductor current peak to peak value

at twice the full-load current, which makes the inductor current go negative in each switching cycle for all load currents. In the QSW topology both the top and the bottom switches turn on at zero voltage which reduces the turn-on switching loss.

The smaller inductor makes the transient response faster. However, smaller inductance also results in large current ripple in the steady-state, which greatly increases the turn-OFF switching loss and degrades the steady-state efficiency. Also, large inductor current ripple causes large steady-state voltage ripple at the output capacitors, which is almost comparable to the transient voltage spikes.

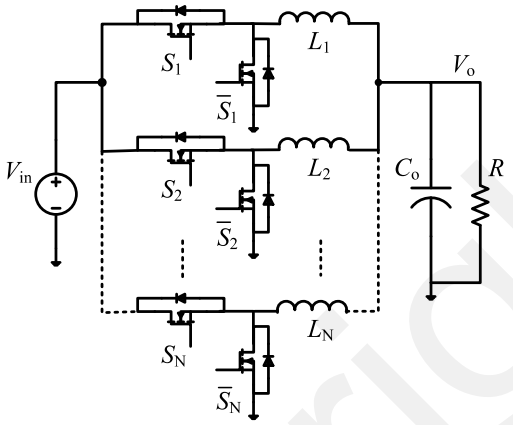

Figure 1.10: Multi-phase buck converter

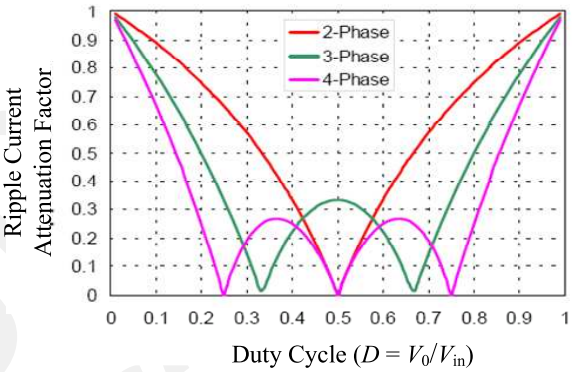

Figure 1.11: Current ripple cancellation at the output capacitor [32]

As the technology grew, the microprocessor operating clock frequency increased for faster computations, which resulted in higher current consumption. It remained no longer practical to use the synchronous buck or the quasi-square wave converter as the VR at higher current due to their limited efficiency and large output voltage ripple. The multi-phase buck converter solution of [28] solves the problem by operating several synchronous buck converters in parallel in a phase-staggered manner. Fig. 1.10 shows the generalized *N–phase* interleaving buck converter, where the output current is the sum of individual phase currents. Phase-interleaving proposed in [32], not only reduces the current ripple at the output capacitors (Fig. 1.11), but also increases the fundamental frequency of the output capacitor ripple current. This in turn reduces the steady-state output voltage ripple, making it possible to use smaller inductors in individual phases to improve the transient response [33, 34, 35]. Since the phase inductances of the multi-phase buck converter are effectively connected in parallel, the slew-rate of the output current increases significantly (compared to a single phase buck converter) during transient conditions, thereby, reducing the out-

put filter capacitor requirement. As a smaller output capacitance is sufficient to meet both the transient and the steady-state requirements, the power density of the VR significantly improves. The interleaving operation decreases the R.M.S current of the input filter capacitor [36] as well, as shown in Fig. 1.12. It also helps in thermal design because of its even current distribution among the phases.

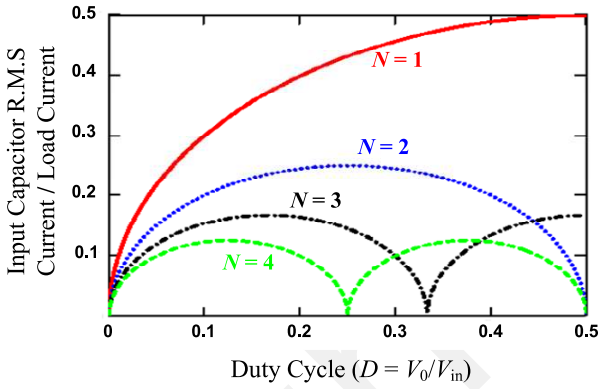

Figure 1.12: Input capacitor R.M.S current of multi-phase converters; N: No. of phases

Even though the multi-phase interleaving buck converter offers current ripple cancellation at the output, the individual inductor current ripple remains the same. The coupled inductor schemes [37, 38, 39, 40] minimize the individual inductor current ripple, thereby improving the steady-state efficiency. The inverse coupled inductor scheme of [37] also improves the dynamic performance by lowering the inductance during transients.

Limitations of the multi-phase buck converter: As mentioned earlier, the future generation microprocessors are expected to operate at sub 1 V level to further reduce their power consumption. The operation of multi-phase buck topology at such low voltages makes the duty cycle extremely small as illustrated in Fig. 1.13 (the duty cycle is 0.08 for 12 V input and 0.05 for 19 V input). The multi-phase buck converter, which is widely used as the VR suffers from the following limitations due to this narrow duty cycle [41].

- Limited controllability due to very short conduction time of the main switch. It is very difficult to operate at high switching frequency.
- The conduction time of the main switch is almost comparable with the switch rise and fall times. Therefore, before the main switch is completely turned ON,

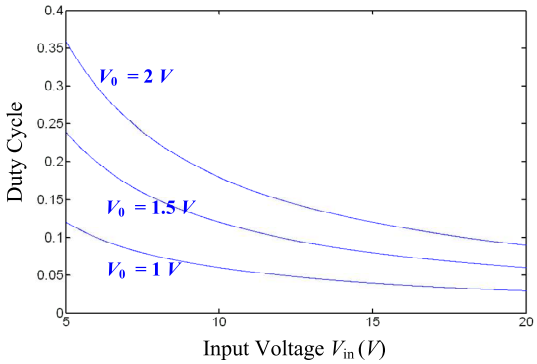

Figure 1.13: Duty cycle vs. input voltage at various output voltages

it must be turned OFF. This makes the main switch to work mostly in the linear region causing significant loss.

- In a buck converter, supplying a fixed output power the main switch average current remains the same. The narrow duty cycle causes the peak value of the main switch current to be large and hence leads to more switching loss.

- With higher input voltage, the phase voltage of the synchronous rectifier switch is high, which results in higher reverse recovery loss of the synchronous rectifier switch.

- With smaller duty cycle, the inductor current ripple becomes larger, which not only increases conduction loss in the inductors but also increases the switching loss of the power MOSFETs. All these incremental losses impair VR efficiency.

- The current ripple cancellation factor at the input and the output capacitors is a function of the duty cycle and the number of phases. From Figures 1.11 and 1.12, it is clear that a smaller duty cycle results in poor current ripple cancellation. More input filter capacitors are needed to filter the high frequency pulse input current and more output capacitors are needed to reduce the steady-state output voltage ripple.

- The time delay in the switching action effects the transient response. Smaller steady-state duty cycle corresponds to larger switching action delays [42] and hence higher transient output voltage spike.

- Sensing the main switch peak current with very short conduction is difficult.

1.2.2 VR Design Challenges

The tight voltage tolerance requirement on sub 1 V output voltage demands large number of filter capacitors, especially with increasing slew-rate of the microprocessor currents. The increase in the number of passive components raises the VR cost. They also occupy significant part of the valuable motherboard space. The problem of low efficiency of the multi-phase buck converter at sub 1 V output, restricts its further use as VR. All these limitations pose stringent challenges for the VR design engineers to develop an efficient, fast and cost-effective voltage regulator for powering the future microprocessors. The following challenges [43] need to be addressed to achieve the desired VR performance.

1. Advanced VR topologies: Alternative topologies have to be introduced to improve the efficiency by extending the duty cycle [41, 44]. The topologies should offer soft-switching with simple gate drive and easy magnetic implementation so that they can be operated at high switching frequencies for high bandwidth.

2. Fast transient response: Voltage regulator modules are typically designed to achieve control bandwidth of 1/10 to 1/6 of the switching frequency, based on models derived from averaging. However, transient response is fundamentally limited by the slew rates, regardless of the control methods employed. High efficiency requirement restricts the VR to operate at a lower frequency which limits its bandwidth [45, 46]. The limited bandwidth has to be compensated with additional bulk capacitors at the output. Minimization of the output bulk capacitors is one of the major challenges, particularly in mobile products like laptops where the space is limited and cheap aluminium electrolytic capacitors cannot be used as in the desktop PC. The concept of adaptive voltage positioning (AVP) helps in minimizing the number of capacitors, where the filter capacitors are chosen to maintain constant output impedance [19, 47].

3. Advanced power architectures: Alternative power architectures have to be developed to completely eliminate the expensive bulk capacitors. Hybrid VR architectures like active-clamp [48], fast response double buck converter [49], active transient voltage compensator [50] etc. use auxiliary circuits to serve the purpose of the bulk capacitor. The main challenge is to optimally use the auxiliary circuit during transients so that it will not affect the system efficiency, particularly with the increasing frequency of the load transients.

4. Advanced control techniques: In a linear compensated controller, the compensation network introduces a time constant which affects the transient response. Non-linear control schemes like hysteretic control [51, 52], V^2 control [53], enhanced V^2 control [54] offer fast response due to non-existence of the compensation network delay. Maintaining constant switching frequency throughout the load variation range is the primary challenge in these control schemes.

5. High performance power devices: Currently, vertical trench MOSFETs are widely used in VR design, whose performance is characterized by its figure-of-merit (FOM). A lot of effort have been made to reduce the FOM by considering alternative power device structures [55, 56]. Device integration and packaging play significant roles in minimizing the interconnection loss and parasitic inductance. Recently developed device integration technology DrMOS [57], packages both the power devices (the top and bottom switches) and the gate driver, together to form a surface-mounted chip. These devices support very high frequency operation for the VR.

1.3 State-of-the-art VR Solutions

A brief literature survey pertaining to the topic of this thesis is presented in this section. The various solutions and a comparison among them are discussed in detail in the subsequent chapter.

The narrow duty cycle associated with high step-down conversion using multiphase interleaving synchronous buck topology as VR results in problems like: lower efficiency, difficulty in sensing switch current, limited controllability and poor ripple current cancellation [41]. To address the short duty cycle problems, several VR topologies [41, 44, 58, 59, 60, 61, 62, 63] have been developed.

A two-stage buck converter [44] uses two buck converters in cascade. This approach gives reasonable efficiency from low to medium current levels. Since the power passes through the two cascaded stages, the efficiency degrades at higher output current due to dominated conduction losses. Hence more number of power switches in parallel or more number of phases in parallel are required to achieve reasonable efficiency. Tapped-inductor buck converter [58] suffers from the voltage spike problem caused by the leakage inductance of the tapped-inductor, poor ripple current cancellation and moving RHP zero. To overcome these problems, active-clamp coupled-buck

converter [59] was proposed, which involves more magnetic circuit complexity. In the non-isolated forward topology [60] the transformer core utilization is poor. Also this topology needs a reset winding or snubber circuitry to demagnetize the core in every switching cycle. Non-isolated push-pull buck converter [61] uses two windings in the primary, which makes the transformer design more critical and it is very prone to transformer saturation. Non-isolated double-ended topologies [62, 63] use smaller transformer turns ratio compared to the isolated topologies. The smaller turns ratio increases the blocking voltage of the synchronous rectifier switch, which raises the reverse recovery loss. In the converter proposed in [61, 63] the pulsed input current flows to the output directly, which increases the steady-state output voltage ripple. The phase-shift buck converter [62] requires a special bootstrap driver.

The stringent transient response requirement of the VR demands lower filter inductor value or more number of filter capacitors to reduce the transient voltage spikes. But it is not practically feasible to add more capacitors due to the cost and the motherboard space restriction. High switching frequency operation helps to reduce the LC filter size but increases the switching loss and needs a tradeoff between fast transient response and high efficiency.

Different techniques have been proposed in order to improve the dynamic performance of VR without affecting the steady state efficiency. The inverse coupled inductor schemes [37] can improve the efficiency without compromising the transient response. However most of the inductor coupling schemes require expensive custom-designed cores. The DC-DC stepping inductance [64] need complex inductor structure and additional snubber circuitry. Reference [65] utilizes a balancing winding to couple the multi-phase inductors without the need for a customized multi-leg core. Although this scheme improves the dynamic performance, still the tradeoff between the efficiency and the transient response has to be made while choosing the value of the coupling coefficient. Quasi-parallel VR [66] improves the transient response by operating an unregulated converter in parallel with the regulated converter. But even number of unregulated converters are necessary to cancel the large output voltage ripple, which increases the number of components. In [67], only the load step-up transient response is improved by using switch-capacitor stage at the input, which is not helpful, as the value of the output capacitance is mainly decided by the voltage overshoot caused by the load step-down transient.

Various auxiliary circuits (hybrid VR solutions) and their control methods [49, 50, 68, 69, 70, 71, 72, 73, 74] for the VR have been proposed to minimize the voltage

overshoots and undershoots during load transients. In [49, 50, 68, 69, 70, 71, 72, 73], there is no control on the amount of current injected/absorbed by the auxiliary circuit during transient conditions. This may cause the auxiliary circuit to inject/absorb more current from the output, which increases the settling time of the output voltage for small and medium load transients. Single shot transient suppressor, mentioned in [68] is theoretically dissipative. The auxiliary circuit in [69] may inject unpredictable currents as the slew-rate of the auxiliary circuit current is decided only by the trace and the switch inductance. The active transient voltage compensator [50] needs complicated transformer design and the performance depends heavily on the power delivery path parasitics. The auxiliary switch control in [71] is very susceptible to the noise caused by the auxiliary circuit switching, as it is controlled using a differentiator on the output voltage. Reference [74] proposed a control scheme to minimize the power loss in the auxiliary circuit. However, the effect of the auxiliary circuit operation on the main converter control loop response was not considered.

1.4 Objectives and Scope of the Thesis

Objective 1: To improve the efficiency of the VR by extending the duty cycle. A simple transformer-coupled VR topology is selected to extend the duty cycle.

Objective 2: To meet the transient response requirement. A hybrid VR architecture is proposed to minimize the number of bulk capacitors at the output.

Objective 3: To optimally utilize the auxiliary circuit of the hybrid VR in order to minimize the dynamic power loss in the auxiliary circuit.

Transformer coupling has been used to improve the efficiency of the VR by extending the duty cycle. But the dynamic performance of the transformer coupled topologies is poor due to their low inductor current slew-rate and the leakage inductance of the transformer. This work proposes two VR solutions to improve the transient response of the transformer coupled topologies.

A 'coupled inductor half-bridge current doubler rectifier (HBCDR) converter' [75] is proposed to improve the dynamic performance of the HBCDR converter with minimal power loss (in the additional circuit) during the transient operation. The coupled inductor uses a balancing winding [65], which can be realized by placing a few turns

on the core of each inductor. Thus coupling of the two inductors is achieved without the need for customized multi-leg core. Both the steady-state and the transient inductances are function of the coupling coefficient 'K' and both will decline as 'K' increases. Although higher coupling reduces the transient inductance for better transient performance, the steady inductance also reduces leading to larger current ripple and lower efficiency. In the proposed converter, the inductor coupling is introduced only during the transients so that the steady state inductance and hence the efficiency remain unaffected by the value of the coupling coefficient. In interleaving buck converters, the load step-down transient is worse than the step-up transient due to lower inductor current slew-rate. In contrast, in the proposed converter, the inductor current slew-rates during the load step-up and step-down transients are almost equal in value, which helps in selecting the optimal filter inductor. The operation, analysis, design and limitations of the proposed 'coupled inductor HBCDR converter' are presented.

The hybrid VR solutions use auxiliary circuits in parallel with the main converter to supply/absorb the unbalanced current at the VR output during transients. Most of the existing hybrid VR solutions (except [74]) have not made any attempt to minimize the power loss in the auxiliary circuit, which affects the system efficiency. As the frequency of the load transients increases, the power loss in the auxiliary circuit during transients becomes a serious concern and needs to be considered. The existing hybrid VR solutions have not analyzed the effect of the auxiliary circuit operation on the main converter control loop response and the energy efficiency of the overall system.

In this work, a control scheme [76] is proposed to minimize both the power loss in the auxiliary circuit and the effect of the auxiliary circuit operation on the main converter control loop response. The chosen hybrid VR consists of an isolated full-bridge current doubler rectifier (FBCDR) in parallel with an auxiliary buck converter. The FBCDR is designed to achieve good steady-state efficiency while the auxiliary buck converter is designed to meet the transient response requirement. The main objective of the proposed control scheme is to improve the energy efficiency of the VR, by optimally operating the auxiliary buck converter during the transient period. The operation, design and verification of the proposed control scheme by simulation and experiment are presented.

1.5 Thesis Outline

The thesis consists of five chapters and three appendices and is organized as follows.

Chapter 1 provides background information on the topic of the thesis. The design challenges for the VR design engineers to develop a highly efficient, fast-acting and cost-effective voltage regulator for powering future microprocessors are discussed. Finally, state-of-the-art VR solutions, objectives and the scope of the present work are outlined.

Chapter 2 presents a brief literature survey on various existing VR topologies and hybrid VR solutions. The advantages and shortcomings of the VR topologies reported in the current literature are discussed. At the end, an introduction to the proposed VR solutions is presented.

Chapter 3 proposes two VR power architectures to improve the efficiency as well as the dynamic performance of the voltage regulator when compared to a standard multi-phase buck converter. The first solution 'coupled inductor HBCDR converter' increases the inductor current slew-rate through inverse coupling of the phase inductors only during the transients. The operation and design of the 'coupled inductor HBCDR converter' is presented with supporting simulation results. Its practical implementation problems are also mentioned. The second solution uses a hybrid VR architecture in which an auxiliary buck converter is operated in parallel with a full-bridge current doubler rectifier converter to supply/absorb the unbalanced current at the VR output during transients. A control scheme is proposed to utilize the auxiliary buck converter optimally as a controlled current source during transients. The operation of the proposed control scheme and the design of the power converter are presented.

Chapter 4 describes the hardware setup and the experimental results from the prototype hybrid VR. Power and control circuit waveforms at steady state are shown first to establish satisfactory operation of the main converter. The experimental results for load current step-down and step-up transients for different cases of operation are presented next along with simulation results. The effect of different operating conditions (i.e., load current step size, load current transient frequency, load current duty cycle and the input voltage) on the VR energy efficiency and the voltage tracking error of the VR is also demonstrated.

Chapter 5 presents the conclusion and limitations of the solution proposed in this thesis as well as future directions of work in this area.

Appendix-A (Detailed control circuit design) gives the hardware details of the control circuit.

Appendix-B (Design of the planar transformer) gives the detailed design of the planar transformer.

Appendix-C (PCB design and layout) discusses important PCB design guidelines for designing a high frequency, high current power converter. The PCB layout designed for the proposed VR is shown.