Abstract

The future generation microprocessors will run at very low voltage (0.8 V), and may consume currents in excess of 150 A with slew-rate greater than 120 A/ns at the CPU die. These impose stringent challenges for the voltage regulator (VR), a dedicated DC-DC converter for the microprocessors, such as maintaining high efficiency while delivering high current and accurately regulating the sub-1 V voltage under very fast dynamic conditions. Multi-phase buck converters is the most widely used VR solution. The operation of multi-phase buck converters at very high conversion ratio results in lower efficiency, limited controllability and poor ripple current cancellation due to associated narrow duty cycle.

Transformer coupled topologies has been used to improve the efficiency of the VR by extending the duty cycle. But they suffer from poor dynamic performance due to 50% duty cycle limitation (to avoid transformer saturation) and also due to the leakage inductance of the transformer. Two VR solutions to improve the dynamic performance of the transformer coupled topologies are proposed.

In the first solution 'coupled inductor HBCDR converter', the HBCDR converter promises improved steady state efficiency with extended duty cycle and the proposed coupled scheme increases the inductor current slew-rate (through inverse coupling) without requiring specialized magnetic core. The effectiveness of the proposed scheme is first analyzed theoretically and then verified by simulation. From the analysis, it is observed, that the inductor current slew-rate is 30 times higher than the conventional HBCDR converter. The practical implementation limitations and its possible solutions are presented.

The second solution uses hybrid VR architecture consisting of a full-bridge current doubler rectifier (FBCDR) in parallel with an auxiliary buck converter. The FBCDR converter is designed to achieve good steady-state efficiency while the auxiliary buck converter is designed to meet the transient response requirement. Even though this solution improves the dynamic response but the dynamic power loss in the auxiliary converter becomes an important issue with increasing frequency of the load transient. A control scheme to minimize both the power loss in the auxiliary converter and the effect of the auxiliary converter operation on the main converter control loop response is proposed. An experimental prototype of the hybrid VR (9∼19V/1V, 30 A, 500 kHz) is built and tested successfully.

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