Abstract

Performance improvement of MEMS based, capacitive comb type accelerometers is presented in this thesis. For this, couple of planar comb structures are developed using two different multi-user/project MEMS prototype processes namely PolyMUMPs (thin polysilicon film based) and SOIMUMPs (thick single crystal silicon on insulator based) from a commercial foundry. As a starting point, arrays of simple polysilicon micro-cantilevers are constructed and analyzed to achieve familiarity, as well as gauge the criticalities of the structure/process before attempting the complex comb devices. The method of polysilicon stacking (up to 3.5μm), together with moderately enhanced aspect ratio possibilities for combs and sense gap was successfully utilized to develop *U*-spring type comb accelerometers having improved capacitances in the range of 10's of *fF* along with mode frequencies upwards of 10*kHz*, within an active area of 500×500μm^2. The above-said implementation was also supported through design, simulation, fabrication and wafer level testing of the devices.

Following this, the sensitivity improvement work utilizing multi-fold springs which are innovatively designed to have reduced stiffness co-efficient and complying with the polyMUMPs process is carried out. Through systematic design and simulation, the comb structures with proposed springs are shown to exhibit comparable (at times better), performance and yet consume lesser area (up to ~7%) as compared to the existing equivalent serpentine spring based comb devices. Fabrication and wafer level characterization of proportionately reduced models of the proposed multi-fold spring based comb structures are also attempted to validate the basic functionality and prove the concept.

Next, the limitations of preceding comb structures mainly of that of small signal to noise ratio and stiction effects is addressed by developing large, robust, high aspect ratio, trench based SOI comb systems. Devices with capacitance in *pF* range (as a result of >12:1 aspect ratio) and 100% stiction-free large areas (4500×3500μm^2) due to backside substrate trenching is designed and successfully implemented using 25μm thick SOI process. Following this, a versatile PGA packaging, PCB based flexible integration (with a commercial capacitance interface circuit) and extensive testing is carried out to establish a consistently working device having sensitivity of ~450*mV/g* and mode frequency of ~2.5*kHz*.

Subsequently, some of the limitations noticed in the afore-said SOI comb devices like, the backside substrate trenching and associated processing are addressed by contriving perforated structures and implementing them in a trench-free way, within the existing frameworks of the above selected SOI process. This proposition was supported through comprehensive design, simulation, fabrication and wafer level testing of simple cantilevers followed by comb structures to ensure their working. This is shown to not only reduce a mask level, but also alleviates the process complexity, resulting in decreased fabrication costs. Finally, the off-chip integration of trench-free accelerometer system is also carried out alike explained prior and its performance presented by comparing with an equivalent 'trench' accelerometer counterpart to complete the study.

Keywords: MEMS Accelerometers, Comb structures, Polysilicon devices, Multi-fold springs, SOI devices, Trench-free method, Perforated cantilevers, etc.