Abstract

This dissertation presents the design of sampled analog VLSI architectures that can be applied to real time signal processing. These architectures consume minimum hardware than their equivalent digital architectures and eliminate the need of data converters by processing input analog signals in terms of discrete time unquantized samples. In this work, several sampled analog architectures have been proposed to implement various useful transforms such as discrete wavelet transforms (DWT) as well as digital signal processing (DSP) algorithms of adaptive nature such as least mean square (LMS) algorithm based adaptive FIR filters. Initially, the design of various sampled analog architectures to implement DWT is presented, where the DWT coefficients are realized by the ratio of capacitors in switched capacitor (SC) circuits and addition and subtraction operations are carried out with SC integrators. In an attempt to realize adaptive circuits, a sampled analog architecture is proposed to implement LMS algorithm based adaptive FIR filter with just half the number of multiplier blocks compared to what is required in its conventional implementation, and the same is applied to realize system identification and channel equalizer architectures. A sampled analog architecture is proposed to implement the signal processing tasks involved in a cochlear implant as a real time application of DWT. Current mode sampled analog architectures are proposed to implement DWT, where DWT coefficients are realized by properly choosing W/L ratios of MOS transistors and intermediate current samples are stored across the gate-to-source parasitic capacitance of the MOS transistors as voltage samples. A detailed study of non-idealities occurring in sampled analog architectures that degrade the performance is presented, where a low complexity model with less number of technology parameters as compared to BSIM3v3 model is proposed to study the MOS transistor switch non-idealities such as channel charge injection error and clock feed through effects.

All the proposed sampled analog architectures are validated through simulations on commercially available 0.18µm CMOS technology. Simulation results show that sampled analog architectures have the ability to implement DSP algorithms with minimum hardware and best suitable for the applications where low cost is of prime concern than the accuracy.

Keywords: Sampled analog, Discrete time, VLSI architecture, Discrete wavelet transform, LMS algorithm, Adaptive filter, Cochlear implant, channel charge injection, clock feed through.