Review of Examiner 2

1. (chapter 1) please clarify about the buffer and channel region in the GaN layer shown in the figure 1.1, schematic diagram of AlGaN/GaN HEMTS page 4.

   Ans: The buffer and channel layer have been specified in the figure 1.1 of AlGaN/GaN heterstructure in section 1.2, page no 4, chapter one. Channel region is the interface of AlGaN/GaN whereas buffer region is the initial layers of Gallium nitride
2. (chapter 2) please mention the estimated Al composition of the 25 nm thick barrier layer estimated from the previous section, in hydrodynamic simulation of AlGaN/GaN HEMT page 22.

   Ans: 30% aluminium is considered in AlGaN barrier layer of AlGaN/GaN structure. This line "The Aluminium composition of 30% is considered in the AlGaN barrier layer" is included in the page no 22, section 2.3 and chapter two of the modified thesis.
3. (chapter 2) please mention the thickness of the SiN passivation layer in Figure 2.4, page 23.

   Ans: the thickness of silicon nitride (SiN) layer is 0.2 micron, which is now specified in the figure 2.4, page 23 of chapter two.
4. (Chapter 2) try to include a discussion to eliminate effect of the higher carrier temperature which creates hot spot and degrades the device performance in the channel region, page 26.

   Ans: Thank you sir for the suggestion. I have incorporated the discussion how to eliminate the hot spot problem in page 26, section 4, and chapter 2 of the modified thesis. Lines are incorporated as "So, we must eliminate this hot carrier effects to improve the device characteristics. By increasing the drain-gate distance, the carrier temperature can be reduced as the electric field will be reduced in the channel region. Also, the bias voltages are required to scale down to reduce the hot spot problem. Apart from that, the field plate technology [91], which is already well accepted, can be used to mitigate the high temperature effects in the channel region. Thermal conductivity of channel layer should also be higher so that the thermal energy can be dissipated through the device surface".
5. (Chapter 3) Polish of language is required in the few parts of the thesis such as "first, the substrate is heated….with N2 plasma ambient for 40 minutes for removing the unintentional oxides and to form three mono layer of AlN"

   Ans: Thank you sir for indicating the issue. We have changed this part in the thesis like this "The substrate is initially heated at 700^0 C temperature in the preparation chamber. After that, nitridation is performed in the growth chamber in N_2 plasma ambient for 40 minutes to remove the unintentional oxides. In this process, two three mono layers of AlN is formed". The modified language is incorporated in page 36, section 3 and chapter 3 of the revised thesis.

6. (Chapter 3) Please correct the units in the table 3.2 for the In cell and Ga cell, page 44.

   Ans: Sorry for the mistake sir. The unit is Torr which is specified in the table to represent the flux of the cell in Table 3.2 of page 44 and chapter 3 of the modified thesis.

7. (Chapter 4) please include the correlation between growth of high In content InGaN in chapter 3 and low In content InGaN interlayer in chapter 4 which is 2%.

   Ans: Thank you sir for the suggestion. The challenges in high Indium incorporation in channel and the correlations between these two chapters are incorporated in page 57, section 4.2 of chapter 4 as "It is difficult to incorporate higher indium composition in the channel region at relatively higher growth temperature. We found that there is a trade-off between the higher indium incorporation and the crystalline quality of the layer. In chapter 3, we have studied the behaviour of InGaN layer on silicon substrate, whereas in this chapter we have grown the AlGaN/InGaN structure on sapphire substrate to achieve superior electrical characteristics."

8. (Chapter please include a schematic diagram of the device and mention about the contact metals used in the study of forward and reverse characteristics, page 83)

   Ans: we have used Aluminium as schottky contact and indium for ohmic contact. The schematic for the device with contact has been included as Figure 5.1 in page 83 of chapter 5 of modified thesis as per your suggestion.