Abstract

COordinate Rotation DIgital Computer (CORDIC) algorithm is an iterative method for fast hardware implementation of vector rotations. The computation of trigonometric functions, coordinate transformations or rotations of phasors and numerous matrix based arithmetic can be efficiently implemented using processing elements performing vector rotations. The CORDIC offers an opportunity to compute all these functions in a rather simple and elegant way. The CORDIC algorithm, originally proposed using nonredundant radix-2 arithmetic, has been refined in terms of throughput and latency with the introduction of redundant arithmetic and higher radix techniques. Recently, there has been a renewed interest in the use of CORDIC algorithm for various applications in biomedical signal processing, neural networks and wireless communication systems to mention a few.

Despite the low area and high latency solutions offered by bit and word serial architectures, unfolded implementations are indispensable where real-time processing with high throughput is required. In this thesis, we propose architectural modifications for unfolded rotational CORDIC algorithm to improve throughput and latency. This has been achieved by reducing the iteration delay and number of iterations. The iteration delay is reduced by using redundant arithmetic and by predicting the directions of all microrotations prior to the computation of rotations. Higher radix number representation is employed to reduce the number of iterations compared to the conventional CORDIC. The design of highly scalable parallel and pipelined architectures with regularity are proposed. The parallel architectures are highly suitable for the implementation of customized hardware in portable devices where large parallelism and low clock rate can be utilized to meet low power consumption requirement. The improvements achieved through

the proposed pipelined architectures are of importance for future embedded high performance processors using large number of CORDIC units for their arithmetic cores.