Abstract: This dissertation has reported two *new classes* of model reference adaptive controller (MRAC) based speed sensorless drives. A fictitious quantity X-based MRAC which is free from integrators and differentiators is proposed for low rotor speed estimation in a vector controlled induction motor drive. This MRAC was found to be stable in all the four quadrants of the torque-speed plane. However, this formulation was dependent on stator resistance (R_s) and hence the accuracy of the speed estimation was sensitive to R_s variation. This explored the possibility to use a different formulation of MRAS to estimate stator resistance if speed is available. The performance of X-based MRAS to estimate stator resistance is reported. Progressing further PY-based MRAS is proposed for stator resistance estimation that does not need speed information. A comparative assessment of different formulation for stator resistance estimation is also presented.

To overcome the stator resistance dependency, another MRAC was proposed based on reactive power exploiting its reference frame independence property. This formulation was not only stable in all the four quadrants of torque-speed plane but also independent of stator resistance and hence could provide better performance at low speeds. To further make the drive insensitive to parameter and load torque variations, the current controllers are replaced by chattering-free second order sliding mode controllers. The performance of such a drive is better than the drive with hysteresis or PI current controllers because constant inverter switching frequency could be maintained and also inherent decoupling between torque and flux is achieved without the need of any parameter sensitive decoupling terms. Also, the dynamics and disturbance rejection properties of such a drive are analyzed thoroughly using sliding mode control theory. The induction machine vector control algorithm along with the proposed estimation and control schemes is simulated using Matlab/Simulink and the results are reported. Also, the propositions are experimentally verified using an FPGA based low cost hardware setup developed in the laboratory.