Abstract

THE PRIMARY CHALLENGE during the modern integrated circuit development process lies in coping with the progressively shorter time-to-market of the chips. Modular design through design re-use in the System-on-Chip (SoC) technology though aids in reducing the design time, the process of testing and verification of such highly complex circuits turns out to be more challenging. The overall objective of this thesis is to bring about reduction in the time-to-market of a SoC development process, by reducing the test time and time to verify the complete SoC for its timing closure.

The design of a generalized reusable core that can perform built-in self-test for logic cores and interconnects, when integrated into a SoC design, has been proposed in this thesis. This core helps in reducing the time taken to design test components in a SoC. An algorithm to find the shortest test set for the random-pattern testable faults in a circuit, by finding the best initial configuration of a given pseudo-random pattern generator, has also been presented. This algorithm targets to reduce the test time by reducing the test data volume. Reduction in test time is further brought about by reducing the test vector application time in sequential cores. A method of parallel application of test data into the internal flip-flops, without increasing the number of test pins, is proposed through the design of an expander circuit. Sufficient reduction in test application time, yet with high fault coverage, was observed from the experimental results. Finally, reduction in the time-to-market is targeted through reduction in the time taken to perform timing verification on a complete SoC design. A hierarchical timing verification algorithm along with a method of clustering, based on timing dependencies among the interface timing paths, is proposed that can bring about considerable reduction in the verification time. The significance of the proposed approaches is demonstrated through experimental results on synthetic SoC designs, generated out of ISCAS benchmark circuits.