Abstract

To alleviate interconnect scaling problem, Network-on-Chip (NoC) has evolved as a standard to design advanced Multiprocessor System-on-Chip (MPSoC). In a NoC, the functional modules (known as Intellectual Property (IP) cores) communicate between themselves using an underlying fabric of routers, connected in some topology. Furthermore, three-dimensional (3D) integration has been proposed recently as an alternative to meet interconnection scaling demands. To design three-dimensional NoC (3D-NoC) based systems, the communication channel across vertical direction of an extended router can be implemented by Through-Silicon-Via (TSV), which are often limited in number. The challenge in combining both the approaches of 3D and NoC is to come up with the association of routers of the 3D fabric with the cores of the application (known as application mapping) and proper placement of limited number of TSVs. The strategy should make efficient usage of the available hardware resources and be able to accommodate all the cores satisfying the communication needs. This thesis reports a number of application mapping and TSV placement strategies for 3D NoC design. Apart from performance, power and temperature have become two other dominant constraints in chip designs. Thermal problems are also exacerbated with the transition from 2D to 3D. To remove heat from stacked silicon layers and alleviate the hotspots, thermal-vias can be utilized. However, thermal-vias consume area and thus increase the IC cost. The thermal challenge can be addressed by judious placement of cores and thermal-vias in the chip. This thesis has proposed a number of techniques to address this problem. Thermal-safety during testing also cannot be ignored. High local temperatures during test may create local hotspots that may lead to chip burn-out, and as a result, yield loss. The variance in temperature across the chip changes the delay of different parts of the chip. This may cause some good chips to fail delay test and/or some bad chips to pass, affecting the yield and quality of products. The thesis has also proposed both exact and huristic method to address the thermal-aware NoC test scheduling problem.

Key Words: Network-on-Chip (NoC), Three Dimentional NoC (3D-NoC), Application Mapping, Through Sillicon Via (TSV), Kerninghan-Lin (KL) Partitioning, Constructive heuristic, Partical Swarm Optimization (PSO), Thermal-aware mapping, NoC Testing.