Abstract

Due to the recent growth in 3G and 4G communication systems the demand of low power single chip wireless transceivers for portable terminals is growing rapidly. To realize the concept of always-on connectivity, the wireless transceiver uses reconfigurable baseband and RF architectures to operate at different standards (GSM, UMTS, WLANs, Bluetooth). This has increased the demand of a high performance digital-to-analog converter (DAC). For high speed applications current steering (CS) architecture is most suitable as it is inherently fast. The conventional segmented CS architecture suffers from several nonidealities and the spurious free dynamic range (SFDR) degrades at higher frequencies.

To overcome the limitations of the existing DACs a new reused distributed binary cells (RDBC) DAC architecture is proposed in this thesis. In the proposed DAC, larger weighted most significant bit (MSB) unit current sources are divided into smaller weighted repeated and distributed binary cells. To validate the proposed architecture, three test chips have been fabricated in National Semiconductor's 0.18 μm CMOS technology which have been tested successfully. The first chip contains an 8-bit 100 MHz low power DAC for reconfigurable baseband transmitters. The power consumption of the DAC is 20.74 mW for 10.06 MHz signal at 100 MSPS sampling rate. Both of the other two test chips contain 10-bit 500 MSPS DACs. Simulation results show that the 10-bit DAC achieves 70 dB Nyquist SFDR even in mismatch environment. To reduce the effect of mismatch a new flexible randomization technique is proposed for the RDBC DAC. A partial foreground calibration technique is also proposed in this work, which improves the linearity of the DAC at a reduced cost. The proposed RDBC DAC achieve improved figure-of-merit (FoM) compared to other reported works.

Keywords- Digital-to-analog converter (DAC), SFDR, dynamic element matching (DEM), randomization, calibration, figure-of-merit (FoM)