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Thesis title: **Design Automation of Analog and Mixed Signal System / Sub-system using Hierarchical Abstraction**

Abstract:

The ever increasing and dynamic requirements of System-on-Chips enforces the reduction of design time of analog and mixed-signal system / sub-system. This can be achieved only by judicious integration of designer's knowledge and cell level circuit design methodologies in the form of a system design methodology. In this research work, a methodology for design automation of AMS system using hierarchical abstraction has been proposed. The methodology utilizes a database of Pareto-optimal hyper-surfaces of the possible constituting cells for optimal design of the system. From system specification, it gives optimally sized spice netlist, ready for physical design. As it may be clear, execution of the methodology needs two preparatory activities. As the first preparatory activity, the AMS system has been hierarchically decomposed into different levels of abstraction, such as sub-system level, block level, cell level, and device level. The second activity includes generation of the Pareto-optimal hyper-surfaces of the possible constituting cells using a combination of epsilon-constraint and geometric programming based sizing method. With this preparation, for a given system specification a top-down design approach has been followed to select suitable topologies of the building blocks and realize them at each level of abstraction. After realizing the building blocks, they are integrated and performance has been verified. Quality of the designed system is highly dependent on the accuracy of the performance of the transistor level cells. Therefore, a special attention has been given for improving circuit sizing methodologies. There are three contributions towards this objective. The existing Sequential Geometric Programming based sizing methodology of analog cells has been improvised to extend its applicability for designing of high performance amplifiers. A new performance parameter, referred to as Effective Second Pole has been proposed to model the phase margin of high performance CMOS operational amplifiers. Also, a methodology of sizing of non-linear circuits like, dynamic comparators, digital gates, and pass switches has been proposed.

The design automation methodology has been deployed to design a number of pipeline ADCs targeting widely varying specification sets (8-10 bit resolution, and 5-100 MSPS sampling frequency). The designed ADCs have been simulated at transistor level. All the designs meet their specification. For each of the design examples, the flow takes about 3-hours to get the final design, ready for layout.

Keywords: CMOS analog integrated circuit; Analog and mixed-signal system / sub-system; computer-aided analysis and design (CAD); Geometric programming; Circuit sizing automation; Performance modeling; Pareto-optimal front; Performance trade-off; Hierarchical abstraction; Topology selection; Pipeline analog-to-digital converter (ADC).