Low power techniques for integrated transceiver subsystem design for wireless sensor node communications

by – Amitava Ghosh (09EC9403)

under guidance of

Prof. Anindya .S. Dhar and Dr. Achintya Halder

Abstract :

Wireless sensor nodes (WSNs) are communication systems that have applications in monitoring different process parameters in an industrial plant, detection and transmission of medical information from a patient to a doctor, rapid communication deployment for military and so on.

WSNs consist of: (i) sensors and data acquisition, (ii) digital signal processing and (iii) radio. The thesis is concerned with designing techniques to reduce the power consumption of the radio section. The power densities of batteries used in WSN are of the order of 100 μW/cm^3 and physical size of the nodes should be kept to a minimum. Hence reduction of radio power consumption is of utmost importance as it consumes maximum power. From the prespective of energy density of the battery, energy consumption of the digital signal processing and radio sections are comparable or latter is greater. The sensor and data acquisition section typically has lower energy consumption than the other two. This is another motivation behind the work in this thesis. Three techniques have been developed for this purpose.

First different modulation schemes have been compared to obtain that binary frequency shift keying (BFSK) is the most energy efficient for short distance communications. Then a variant of BFSK has been proposed that provides first order frequency drift cancellation through differential encoding and detection at the transmitter and receiver respectively. This enables lower power oscillator design at the transmitter side with very little increase in power at the receiver due to differential detection occurring at baseband.

Next, a frequency calibration methodology, architecture and circuit have been designed. The entire design is clocked at the reference frequency rate that helps to reduce power. Calibration time is also moderate owing to the use of fractions instead of integers to determine the frequency, when the oscillator frequency is divided by a reference frequency.

Finally, a transmitter has been designed that uses one-stage ring oscillator for ultra low power consumption. One-stage ring oscillator consumes lowest power within ring oscillator topology. Also since the output is square, buffer power consumption is relaxed. The transmitter draws an average current of 175 μA from 1.6V supply.