Abstract

Of late, there is a steep rise in the usage of handheld gadgets and high speed applications. VLSI designers often choose static CMOS logic style for low power applications. This logic style provides low power dissipation and is free from signal noise integrity issues. However, designs based on this logic style often are slow and cannot be used in high performance circuits. On the other hand designs based on Domino logic style yield high performance and occupy less area. Yet, they have more power dissipation compared to their static CMOS counterparts. As a practice, designers during circuit synthesis, mix more than one logic style judiciously to obtain the advantages of each logic style. Carefully designing a mixed static Domino CMOS circuit can tap the advantages of both static and Domino logic styles overcoming their own short comings.

We propose a methodology based on unate decomposition to realize a mixed static Domino circuit. We present an algorithm for decomposing a Boolean circuit into unate and binate sub blocks. Using an Influence table approach, the decomposition algorithm obtains the maximum unate set, containing states that can realize a Domino block. Later we attempt to find an optimum part of the unate set to be realized using Domino logic and the rest to be realized using static logic.

Next, we present a novel on-the-fly mapping technique to map the obtained Domino block. We follow a node by node incremental mapping approach combining the nodes based on their functional properties. This is done till the restrictions on height and width of the individual cells are reached. Then by re-ordering of cells selectively, we try to gain advantage in terms of delay and minimizing area penalty. We use a two-objective optimization method to find the optimum set of re-ordering cells.

Finally, we propose a power aware clock gating approach for the Domino blocks of a circuit which reduces the dynamic power dissipation of the blocks. We obtain a set of favorable gate patterns which can yield power savings, when clock gating is applied. These gate patterns, in groups are used to match the circuit using sub graph matching algorithm. We try to find an optimum pattern set which gives maximum power savings with a minimum penalty on area. Our proposed methodology is implemented and tested on the standard ISCAS and MCNC benchmarks. Comparative study with the existing works shows that our approach offered 15% improvement in power, 12% improvement in area and 19% improvement in delay.

Keywords: Unate decomposition, mixed CMOS synthesis, cell-reordering, on-the-fly mapping, sub graph matching, clock gating, low power design