ABSTRACT

In bus based Systems-on-Chip (SoCs), due to many on-chip communication challenges, the performance, speed, and power consumption of a system can get affected severely. Network-on-Chip (NoC) has evolved as an alternative that overcomes this bottleneck for integrating large number of cores on a single SoC. The cores communicate with each other using a router based packet switched network. NoC can be designed using either regular or application-specific topologies. Although standard topologies are simple in nature, they might not be the best choice for specific applications, due to mismatch between the topology and the application characteristics. This leads to the design of Application-Specific-Network-on-Chip (ASNoC). With advancement in technology, integrating several different applications into a single SoC has become cost-effective. Such NoC architectures should closely match the traffic characteristics and performance requirements of different target applications. Since different applications have different functionalities, the inter-core communication characteristics can be very different across the applications. Consequently, a NoC that is designed to run one application may be sub-optimal for others. This leads to the need of reconfigurable NoC design that can provide network topology reconfiguration across the applications to satisfy the requirements of currently running application. This thesis reports a number of efficient design techniques for application-specific and reconfigurable NoCs. Need of integration of core selection with application mapping has been presented and a Particle Swarm Optimization (PSO) based approach has been designed for the same. A flexible router placement based ASNoC synthesis has been presented. For this, an exact method based on Integer Linear Programming (ILP) and a PSO based method have been proposed. Another variant of ASNoC synthesis with the integration of floorplan generation has been presented. A PSO based solution has been proposed for the integrated problem and an efficient algorithm for secondary router placement in the floorplan has been proposed. From reconfiguration point of view, this thesis proposes two reconfigurable NoC architectures and configuration policies for them. The first architecture provides reconfiguration in the connection pattern between cores and routers by embedding multiplexers, while the second architecture achieves reconfiguration between the routers by inclusion of configuration switches. Area overheads of the proposed architectures have been shown to be very minimal. The reconfiguration policy works in two phases, namely, mapping of all cores across all applications, followed by application-specific reconfiguration. Two methods – an ILP based exact one and a PSO based method have been proposed for both the phases. An iterative reconfiguration heuristic has also been proposed for the reconfiguration of multiplexer based NoCs. Our approaches have been evaluated taking real benchmarks and compared with the techniques presented in the literature. Simulation results show significant improvements in static and dynamic performance metrics, establishing the superiority of our approaches.

KEY WORDS: System-on-Chip (SoC), Network-on-Chip (NoC), Core Selection, Application Mapping, Mesh, Integer Linear Programming (ILP), Particle Swarm Optimization (PSO), Application-Specific NoC (ASNoC), Floorplan, Sequence Pair, Reconfiguration.