

Abstract

Very exciting and promising results from recent development in group IV alloy films (viz., SiGe, SiGeC, and strained-Si on relaxed SiGe buffers) have led to the belief that SiGe-based devices will open up an entirely new dimension to the future of VLSI/ULSI in Si technology. With the progress in SiGe technology, fabrication of high performance SiGe-HBTs has become feasible. The present work is concerned with the development of strained SiGe material parameter models, modelling and simulation and applications of SiGe-HBTs.

IC design based on SiGe-HBTs requires a physical device model for circuit simulation. Comprehensive analytical models for important strained SiGe material parameters have been developed with device design and optimization in mind. The models have been incorporated in a commercially available device simulator for simulation of SiGe-HBTs and the simulation results have been validated with experimental device data. The way in which dc and ac simulation can be utilized to optimize the high frequency performance of transistors has also been considered.

Both drift-diffusion and energy balance models have been used to optimize the SiGe-HBT design and their suitability for modelling scaled devices has been studied in detail. Extraction of transit time components in a state-of-the-art SiGe-HBT has been taken up. Due to its prospect for low power and high performance in SiGe-BiCMOS technology on SOI, the high frequency performance of lateral bipolar SiGe-HBTs has been studied using simulation.

To develop compact model for SiGe-HBTs, vertical bipolar inter-company (VBIC) model has been applied. A methodology to extract and optimize the model parameters for the VBIC model has been developed. VBIC model parameters have been extracted from dc/ac measurements of SiGe-HBTs and verified and optimized using a VBIC pseudo-code. A comparison has been made to study the suitability of the VBIC and SPICE Gummel-Poon (SGP) models when applied to advanced SiGe-HBTs. Design and fabrication of a SiGe-HBT RF amplifier have been taken up. Finally, planar inductors have been fabricated and characterized on conventional low-resistivity silicon substrates. The technique involves formation of porous-Si and oxidation and pattern transfer oxidized porous-Si.