Abstract

System-on-chip (SOC) design testing becomes a challenging task due to embedded cores and their integration level. In addition SOC may contain different types of cores (digital, analog, and memory) having different test methodology. This leads to the testing of $SOCs$ more critical. Many researches have been devoted to the development of the test techniques for an SOC. But, most of these techniques deal with only testability issues for a homogeneous SOC. The current thesis introduces a new design for testability (DFT) technique for heterogeneous SOC designs. The main objective of the thesis is to address the test challenges faced by an SOC designer. The objective is met by implementing a common or generic test technique for managing the test operations of diversified embedded cores, including 1149.4 wrapped, $P1500$ wrapped, and $BISTed$ memory cores. The present test technique provides high flexibility, low pin-count overhead, and low area overhead which helps the designer to implement this technique with less effort. The developed techniques have been integrated on to a systematic methodology for the testing of SOC design with the help of a computer aided test tool. The technique consists of several techniques to support test vector generation, test scheduling, test set preparation, test access mechanism design for embedded digital, analog and memory cores. Extensive experiments on benchmarks based on $ISCAS'89$, $ITC'97$, and $ITC'02$ SOC test benchmarks resulted in significant reduction of testing time and area overhead. These experiments demonstrate that the present test technique allows to test digital, analog, and memory cores in the $SOCs$ on the same platform.