ABSTRACT

The design and testing aspects of Programmable Lgic Arrays (PLAs) have been studied. An in-depth analysis has been made on the conditions for the detection of all possible types of faults, particularly, the bridging faults and some fruitful conclusions have been drawn. An easily testable PLA with an extra m-bit shift register, acting as a product line selector, is considered and an improved algorithm for testing has been developed where values of don't-care literals are assigned properly to increase the probability of detection of bridging faults.

The PLA is then augmented further with some extra pass-transistors and modified test generation algorithms have been developed which covers 100% faults for the 56 benchmark PLAs with reasonably less testing time. It is shown however that, with this augmentation, 100% fault coverage cannot be ensured, in general. The above PLA is further augmented by adding one or two extra product line(s) with crosspoint devices at proper crosspoints to obtain a new PLA which is fully testable. Two different approaches for ascertaining number of product line required and placement of crosspoint devices are used. Further, a nearly fully testable PLA is proposed in which no extra delay in normal circuit operation exists.

A parallel testing technique for PLAs has been developed, in which the multiple product lines are sensitized during testing. With this technique, the testing time for PLAs is reduced

drastically. It has again been shown, by three algorithms – heuristic, probabilistic and cross-point_device_counting, that the testing time is reduced further by using some sort of ordering the product terms before generating the test vectors. Further, the product lines are efficiently grouped to reduce the extra hardware requirement and the complexity of multiple path sensitization. Besides these, a fully testable PLA is obtained with further reduced extra hardware (in comparison with the previously mentioned fully testable PLA) which can also be tested in very small time.

Two built-in self-testable (BIST) PLAs have been proposed. The first one is based on the crosspoint_device_counting in an interleaved manner; and the second one is based on grouping of product lines and testing by pseudo-exhaustive test pattern generation. In each of the techniques, the reduced test set is obtained and the fault coverage is extremely high. A concept of fully testable BIST PLA has been introduced for the second technique that very small amount of extra hardware. This PLA can also be tested in reduced time.

Keywords:

Programmable Logic Array (PLA), Logic Design, VLSI Testing, Fault Detection, Fault Model, Design-for-Testability (DFT), Easily Testable Design, Testing Algorithms, Parallel Testing, Pseudo-Exhaustive Testing, Built-in Self-Testable (BIST) Design.