Abstract

For an ADC to be used in LMDS receiver, it must show a bandwidth ≥ 550MHz while the resolution should be typically 8-bit. Because of the high trans-conductance, large current drive, low I/f noise, high bandwidth and uniform turn on voltage, HBTs are predominantly used in ADCs operating in gigahertz range. Considering the trade-off between the speed and resolution, the preferred architecture of the ADC for the LMDS receiver application is the folding-interpolating architecture. Therefore, by using 0.25µm SiGe:C BiCMOS technology, an 8-bit, 2.5GS/s Folding-Interpolating ADC (FI-ADC) has been designed. The simulation result of this FI-ADC shows an ENOB of 7.55 at a sampling speed of 2.5GHz and input signal frequency of 600MHz. The total power consumption by this FI-ADC is 2.13W for a dual power supply of 3.8/3.0V.

For the UWB application, an ADC should show a resolution ≥ 4-bit with a sampling speed ≥ 500MHz. The most important requirement of this ADC is that the power dissipation must be low. To achieve the desired targets, a new topology of an ADC, named as Switched Reference ADC (SR-ADC) has been proposed where the reference voltages are applied through switches. The switched reference voltage concept works with few mutually exclusive switches which are appropriately selecting the reference voltages for comparison with the input signal. This SR-ADC has been implemented using 0.18µm CMOS technology. The designed SR-ADC shows an ENOB of 3.53 at a sampling speed of 500MHz and input signal frequency of 100MHz. The total power dissipation is 21.39mW for a power supply of 1.8V.

To improve the resolution of the designed ADCs, the noise minimization of the building blocks (THA, comparator, etc.) has been done before the final integration. For doing the noise analysis of the THA used in FI-ADC, noise correlation matrix has been used where as nullor based models have been used for analyzing the noise associated with the THA used in SR-ADC. The noise and error analyses of the latched comparators have been done through circuit analysis.

Keywords: LMDS, UWB, FI-ADC, HBT, SR-ADC, THA, ENOB.