Abstract

The present investigation elucidates the growth and deposition of ultrathin gate dielectrics such as oxides, nitrides and oxynitrides directly on strained epitaxial SiGe films at a low temperature using microwave plasma for possible VLSI/ULSI applications.

Strained SiGe layers with different Ge concentrations (x = 0.09, 0.18 and 0.26) grown using a Gas Source Molecular Beam Epitaxy system have been used in the present investigation. Detailed epitaxial and compositional characterization of the films have been carried out using Ion Channeling, Rutherford Backscattering Spectroscopy, X-ray Photoelectron Spectroscopy, Spectroscopic Ellipsometry, Atomic Force Microscopy and High Resolution X-ray Diffraction techniques.

An electrodeless microwave oxygen plasma has been employed for the low temperature oxidation of strained epitaxial $Si_{1-x}Ge_x$ films. X-ray Photoelectron Spectroscopy analysis of the oxide layer has revealed the formation of a mixed oxide of SiGe without any Ge pile-up at the oxide/substrate interface. The electrical and interfacial properties of oxide films have been studied using C-V, G-V and I-V measurements. An *in situ* hydrogen plasma treatment of SiGe samples prior to oxide growth is shown to be very useful in improving the electrical properties of the oxide. Post-oxidation and post-metal annealing have resulted in low values of fixed oxide charge density and interface state density.

Nitridation of Si(100), Ge(100) and SiGe has been performed using microwave ammonia plasma. Si has been found to be selectively nitrided while Ge remained in its elemental form. Nitride films have also been deposited on SiGe by microwave plasma assisted decomposition of HMDS in the presence of ammonia and nitrous oxide. The properties of grown/deposited films have been characterized for both the chemical and electrical properties.

Microwave plasma technique has also been used for growing ultrathin gate quality oxides both on Si and SiGe using N_2O. The oxides grown in N_2O plasma have exhibited excellent electrical properties due to incorporation of nitrogen at the oxide/substrate interface. The hole confinement in the SiGe well has been demonstrated by both C-V measurement and simulation. The design trade-off for SiGe-channel p-MOSFETs has been studied. The confinement of the carriers in the SiGe well as a function of the Ge concentration, the width of the SiGe well, the thicknesses of the Si cap and the gate oxide has been studied using a 1-D Poisson solver.

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