Abstract

With the advent of aggressive downscaling in the semiconductor industry, concerns have been raised about the reliability issues such as, device life time, degradation, leakage current and increased defects. Possible remedies are being sought to overcome these issues via use of alternative channel materials, high-k gate dielectrics, and non-classical device architectures. Noise is a fundamental threat to down-scaled devices which needs more attention. The low-frequency noise characteristics reveal many of the information regarding life-time, leakage conduction mechanisms, defects and traps of devices. In this work, the low-frequency noise characterization has been performed on small-geometry devices for device reliability assessment and life-time prediction. High frequency noise measurement has been performed for the evaluation of noise figure and modelling of channel noise in advanced MOSFETs.

A wide variety of novel metal-oxide-semiconductor field-effect transistors (MOSFETs) devices that are contenders for use in future high-speed and low-noise RF circuits have been evaluated. The devices include (i) Strained-Si channel n- and p-MOSFETs on SiGe buffer layer, (ii) tri-gate FinFETs, (iii) gate-all around FinFETs on buried oxide and for reference, Si-MOSFETs. The low-frequency noise has been characterized for different types of operating conditions with different gate and drain bias. Detailed analytical studies have been used to understand the effect of device architecture, strain, device geometry, gate oxide charge and traps, electrical stress-induced degradation on $1/f$ noise. The locations of the dominant noise sources as well as their physical mechanisms were investigated from time domain random telegraph noise (RTN) study. Towards further understanding of the physical mechanisms, inelastic electron tunneling spectroscopy was used to study the different modes of lattice vibrations and phonons. Effect of strain has been analyzed and mathematical models are developed to study the effect of strain on lattice dynamics. Effects of electrical stressing on phonons of different materials have been studied. Trap information including their location and energy were extracted using inelastic tunnelling spectroscopy which has been correlated to the findings of low-frequency noise study. A comparative study on the reliability and device degradation has been performed between planar bulk and strained devices.

Keywords: MOSFET, strained-Si, FinFETs, $1/f$ noise, low-frequency noise, random telegraph noise, electrical stress, phonons, number fluctuations, trap, noise figure, inelastic electron tunneling spectroscopy, lattice dynamics, optical and acoustic phonons.