ABSTRACT

GaAs is considered as a novel channel material in complementary metal-oxide-semiconductor (CMOS) technology to replace Si due to its high electron mobility. However, unlike SiO_2 on Si, formation of poor quality native oxides, such as As-O and Ga-O between gate dielectric and GaAs is the major obstacle in realizing GaAs based MOS devices. Thus interface passivation is a prerequisite before dielectric deposition. In this thesis, the effect of interface passivation on the electrical characteristics of GaAs based MOS capacitors were investigated. Surface passivation of GaAs wafers was done by sulfur, and MOCVD grown epitaxial ZnO (1.8 nm) and InP (1.5 nm) layers. GaAs MOS devices were fabricated using ZrO_2 and TiO_2 high-k dielectric materials. The high-k/GaAs interface was studied by X-ray photoelectron spectroscopy (XPS), deep level transient spectroscopy (DLTS), and high-resolution transmission electron microscope (HRTEM). XPS spectra confirmed the reduction of Ga-O and As-O from the interface between high-k and GaAs in passivated samples. As a result low values of interface trap density (D_{it}) and hysteresis voltage are observed. In sulfur and ZnO passivated devices, the D_{it} and hysteresis voltage is found to be 7.5×10^{11} $eV^{-1}cm^{-2}$ and 0.15 V, and 2.5×10^{11} $eV^{-1}cm^{-2}$ and 0.13 V, respectively, whereas, for InP passivated devices, it is 1.1×10^{11} $eV^{-1}cm^{-2}$ and 0.008 V, respectively. The frequency dispersion for sulfur, ZnO and InP passivated devices were found to be 2.0%, 1.0%, and 1.3% per decade, respectively, when the frequency was varied from 10 kHz – 1 MHz. The ZnO and InP passivated GaAs MOS devices exhibit a higher breakdown time of 1703 s and 1748 s, respectively, compared to 928 s for unpassivated devices. It is found that to passivate the GaAs surface, InP is better than sulfur and ZnO passivation and also compatible with present day GaAs based III-V fabrication technology as both the GaAs and InP materials belong to III-V. As an application, GaAs MOS based non-volatile memory (NVM) devices were fabricated and characterized. MOCVD grown 5 nm InP quantum dots (QDs) were embedded as charge storage elements between high-k control and tunneling dielectric layers, both being ZrO_2. The maximum memory window for this device was found to be 6.3 V and negligible change in memory window without InP QDs indicates that the charge storage into the device was due to the InP QDs. These devices exhibit ~84% charge retention even after 10^5 s. Thus the use of metallic nano-particles as charge-storing element can be avoided in future to prevent metal/oxide interaction, metal or source-drain-gate dopant diffusion during high temperature device processing, and the problem of integration with the current device process technology. The programming and erasing operations are discussed with proposed band diagram.

Keywords: Metal-oxide-semiconductor, GaAs, surface passivation, quantum dot, memory device.