DESIGN OF MULTI-MHz DC-DC BUCK CONVERTERS WITH ACTIVE PHASE COUNT FOR APPLICATION PROCESSORS

Abstract

With the rapid advancement of technology scaling, modern application processors (APs) are implemented in lower technology nodes, featuring a larger number of cores that operate at higher clock frequencies, ultimately leading to a higher average power demand. Additionally, it requires a tightly regulated supply, even at an unprecedented load slew-rate of 1 A/ns during mode transitions such as sleep-to-active modes and vice-versa. For power-performance optimisation, dynamic voltage scaling (DVS) is also required over a wide range with an accurate and fast reference tracking feature. However, the battery, which is the primary power source, cannot directly meet these stringent requirements. Therefore, a multi-MHz DC-DC buck converter with active phase count is used to bridge the gap between the battery and the APs.

This thesis proposes a frequency-synchronised, reconfigurable, current-mode, DC-DC buck converter for powering modern APs with a wide input/output range supporting DVS reference tracking. The frequency synchronisation range of the converter is extended to operate it at 20 MHz. A parameter- and parasitic-sensed critical duty detector is incorporated to enable accurate peak/valley mode transitions at the actual critical duty in closed-loop operation. Next, an efficiency-driven optimisation methodology is proposed for multiphase DC–DC converters to obtain the size of the power MOSFETs in each phase for improving efficiency flatness across a wide load range. A parasitic inclusive, analytically predicted phase current distribution technique is proposed to prevent arbitrary phase currents in unequal phases, eliminating the issues of inductor current saturation and hot-spots in IC. Furthermore, a 1-cycle symmetric output slew-sensed active phase count control with a large load transient predictor is proposed to meet slew-rate of 1 A/ns. This technique activates/deactivates all phases to quickly charge/discharge the output capacitor, achieving a fast recovery. Finally, DVS operation is extended to a multiphase converter through a dynamically referenced, fixed-current-windowing, slew-enhanced APC control technique. This architecture maintains a flat efficiency profile across a wide output voltage range while ensuring fast transient response, making it well-suited for powering next-generation APs.

Keywords: DC–DC buck converter, current-mode control, active phase count, dynamic voltage scaling, multiphase converter, phase current distribution, fast transient response.