

## Abstract

*Automation of the design of analog circuits has long been considered a difficult problem. Typically, analog design requires specialized knowledge, design skills and rich experience for topology selection, trade-off analysis and sizing of circuits. The presence of multiple, conflicting performance objectives along with high sensitivities to parasitics and higher-order device effects makes even the task of sizing a given topology non-trivial. Therefore, efficient CAD techniques are required for improvement of productivity and quality of analog circuits.*

*The work presented herein aims to develop algorithms and CAD tools for performance optimization and design space exploration of analog circuits. A Genetic Algorithm based optimization algorithm is used, where the different cost criteria can either be combined into a single objective function to find a unique solution, or they can be handled by multi-objective optimization methods to produce trade-off solutions on a pareto front. This work also proposes methods for including yield in the design space exploration framework at low computational costs while not sacrificing the accuracy of yield estimates.*

*Towards the goal of developing efficient optimization and design space exploration algorithms, this work contributes in the following ways: 1. A pruned partially ordered graph based representation of the circuit domain knowledge and experience of the relative importance of its different performance objectives, and the use of this graph for determining weights in the composite scalarized objective function. 2. Methods for dynamic adaptation of the weights in the above scalarized objective function during the run-time of the optimization process. 3. An objective function space partitioning based strategy for mixing local and global competition in a multi-objective optimization framework to improve the diversity and quality of solutions on the design decision surface. 4. Method for low-cost but reliable yield estimation using dynamic performance regression models to find yield-performance trade-offs for circuits. Practical circuit examples were taken from three different classes of analog circuits built in an industry-standard 0.18 $\mu\text{m}$  CMOS technology to show the generality of the proposed methods. Encouraging results were found upon application of the proposed algorithms and techniques to these examples.*