Abstract

Modern processors used in data centers and automotive platforms operate under rapidly changing load conditions, requiring voltage regulator modules (VRMs) that can ensure fast and accurate voltage regulation. To reduce distribution losses and minimize the number of power conversion stages, the industry is transitioning from 12 V to 48 V bus architectures, increasing the demand for compact, efficient, and high-bandwidth VRMs. A commonly adopted solution involves a cascaded power architecture, where a fixed-ratio intermediate bus architecture (IBA) is followed by a tightly regulated Point-of-Load (PoL) converter. While regulated IBAs offer benefits in modularity and scalability, they also introduce additional sensing and control challenges, particularly under high-frequency digital control implementations. The Series-Capacitor Buck (SCB) converter has emerged as a promising PoL candidate due to its reduced device stress, automatic current balancing and improved bandwidth capability compared to conventional multiphase buck converters. However, the lack of a comprehensive digital current-mode control (DCMC) framework and robust stability analysis for the SCB, along with limitations of conventional continuous-time (CT) average models in capturing sampling delays and fast-scale instabilities, present key challenges in the modeling and control of digitally operated cascaded architectures.

This thesis proposes the design, implementation, and stability analysis of a digitally controlled cascaded architecture that combines a regulated IBA stage with a DCMC-operated SCB converter. Discrete-time (DT) models are developed for fixed-frequency DCMC, and system stability is further enhanced using an event-based variable-frequency control strategy. To improve transient performance, a multivariable control framework is proposed, exploiting the additional control degrees of freedom in the SCB topology. Furthermore, a digitally phase-shift-modulated (PSM) hybrid switched-capacitor converter is introduced as the IBA stage, with the SCB integrated at the final stage. The complete modeling

framework, controller design methods, and implementation guidelines—including impedance interaction and parameter variation considerations—are validated with simulations and experimental results, demonstrating high-bandwidth, stable operation suitable for 48V-to-PoL applications.

Keywords: intermediate bus, point of load converter, series capacitor buck, digital controller, discrete time model, fast-scale stability, current mode control.