Abstract

Testing is commonly practiced to determine whether any fault exists in a system. Particularly, in the system-on-chip(SOC) design testing is a challenging task due to embedded cores and their integration levels. Much research has been devoted to the development of advanced test techniques and methods to support Design-For-Test(DFT). However, most existing DFT techniques deal with only testability issues but not with the implementation. The current thesis introduce a new DFT technique for system-on-chip(SOC) designs.

The main objective of this thesis is to address the test challenges faced by the designer at the system-level while providing the support by offering choices based on the trade-off between the test hardware and testing time. The objective is met by developing a generic method to provide alternative efficient test solutions for SOC which help the designers to analyze based on the specifications of the SOC designs and choose one for implementation.

The developed techniques have been integrated on to a systematic methodology for the testing of SOC design with the help of a computer aided test tool. The methodology consists of several techniques to support test vector generation. test scheduling, test set preparation, test access mechanism design for analog and mixed-signal cores.

Extensive experiments on benchmarks based on ISCAS'89 and ITC'02 SOC test benchmarks resulted in significant reduction of testing time at the system level and achieved high fault coverage. Experiments conducted on ITC'97 benchmarks demonstrate that the test scheme allows to test digital, analog and mixed signal cores in the SOCs on the same platform.