Contents

List of Figures

List of Tables

1 Introduction

Forward error correction (FEC) codes play a fundamental role in ensuring efficient use of the available spectrum by all modern communication systems. Shannon demonstrated the performance limits of channel coding and modulation schemes in his pioneering report [1]. It was theoretically established that a reliable communication could be possible with a data rate lower than the *channel capacity* by designing appropriate error correcting codes (ECC). However, the landmark work gave hardly any indication of how to construct such practical codes. Ever since then, coding theory experts have endeavored to design codes approaching the Shannon channel capacity limit. In search of powerful error correcting codes, historically several complicated decoding algorithms have been proposed whose hardware realization was found difficult due to high computational complexity of the decoding algorithms. However, the advent of high performance VLSI technologies in the last decade has been able to overcome these difficulties. Efficient hardware implementation of highly complex digital architectures and systems has been facilitated with the ongoing progress of VLSI technology. Thereby, high throughput, low latency and relatively lower energy consumption can be accomplished by exploring the design space carefully. The design of a practically feasible decoder that nearly approaches the Shannon limit has become a thrust area for research. Especially, the high throughput requirements from a large number of emerging services involving data communication have posed a lot of design challenges to be addressed.

This introductory chapter starts with identifying the challenges encountered while trying to implement a high throughput turbo decoder. The need of limited power consumption, reduction of size of memory blocks and high speed of computational kernel are highlighted. Next, the motivation of the present work is clearly spelt out. The chapter ends by giving the outline of the thesis.

1.1 Turbo Code and Its Realization

Turbo code has been able to combine structured codes to closely achieve the limit on channel capacity prescribed by Shannon. Research on turbo codes has witnessed a significant increase in power efficiency as compared to the earlier block and convolutional coding methods. The very first implementation of turbo code used two recursive systematic convolutional (RSC) encoders connected in parallel and separated by a pseudo random interleaver [2]. Iterative decoding method for turbo code has been an important milestone in the progress of communication system design. Because of their outstanding performance, various standards such as 3GPP, IEEE 802.16d and IEEE 802.16e have adopted turbo codes as their channel coding schemes. The turbo principle is being added to an increasing array of applications as well as more and more telecommunication standards worldwide.

Turbo codes have been proven to be an excellent technique for providing substantial increase in bandwidth efficiency in communications over satellite. They have been selected for their impressive forward error correcting capability to regenerate the weak signal on the up link to the satellite. The digital video broadcasting (DVB) system for digital television services makes use of the satellite communication links. In this type of communication channel, turbo codes have been chosen for the return channel via satellite for the additional services of Internet and data transfer.

In deep space communication, turbo codes were selected for their outstanding performance in improving power efficiency over that of the existing codes. It has been considered further for many space exploration projects for their channel coding standards. The important role of turbo codes and their classes is more likely to prevail in all future space projects [3].

Demand of higher capacity of modern data storage systems can be made by increasing the storage density and the data transfer rate. Coding and signal processing efficiently improve the storage capacity in hard-drive systems and magnetic recording channels [4]. The optimal decoding and equalization exhibit a robust and efficient means of faithful reproduction of digitally stored data [5]. Turbo decoding and equalization are therefore becoming the most potential candidate for the next generation read channels in magnetic and optical storage media.

The principle of iterative decoding has been successfully extended to the channel equalization problem [6]. This can efficiently mitigate the impairments, for example, inter symbol interference (ISI), fading and non linear distortion experienced in many communication media.

Turbo codes can be efficiently implemented with Application Specific Integrated Circuit (ASIC) tools in order to accomplish high performance and speed and to satisfy the need of adequate on-chip memory. Turbo decoder used in the portable and hand held devices demand a low power consumption due to the limited battery power. Standard cell based full custom ASIC design offers [7] excellent speed factor while consuming little power and chip area compared to the configurable computing machines (CCM) [8]. It is possible in ASIC to realize a low power, high speed turbo decoder that satisfies the real time constraints of modern telecommunication standards like 3GPP-LTE. Consequently, the ASIC tool has been used in the present work as the target technology for the proposed designs.

1.2 Motivation behind the Present Work

Voice communication is slowly giving way to wireless Internet service. There is a growing demand of newer services by increasing the number of mobile users in the present rapidly changing world. Extremely efficient use of resources like bandwidth and power is becoming the main concern for the designer. It is imperative to design and develop a spectrally efficient capacity approaching code for error free transmission. However, the coding gain required in achieving the Shannon limit [1] comes at the expense of considerable complexity of the decoder. Energy consumption associated with implementing the decoder thereby has become a significant and crucial factor specifically for the wireless system [9].

The invention of turbo codes has triggered a significant amount of research, leading to numerous enhancements and refinements of the originally proposed scheme. Though turbo code offers good performance at low SNR, the large decoding latency due to the iterative execution of typically long data frames creates a major problem in high throughput applications [10, 11]. Efficient architectures like parallel processing [12] offer viable solution by reasonably enhancing the decoding throughput. Hence, there is a need to undertake research towards developing parallel turbo decoder architecture that ensures high throughput while involving reasonably low area and low power consumption.

The design of the interleaver has been deeply investigated, yielding good permutations that substantially improve the distance properties that play a crucial role in achieving good performance of the iterative decoder. Design of efficient interleaver architecture for parallel turbo decoder requires high memory bandwidth to support concurrent access of soft information which, however, is prone to result in considerable power dissipation. Moreover, design of collision-free interleaver for parallel turbo decoder is considered a major challenge in ongoing research. Interleaving permutations that substantially improve the minimum distance property and are suitable for parallel architecture constitute an active research area. Consequently, there is a growing need to develop contention free interleavers which not only provide high throughput but at the same time ensure low power consumption.

Parallel architecture of the turbo decoder can be augmented by pipelining various components of the decoder to further enhance the processing speed with tolerable additional area overhead. So it would be worthwhile to carry out research on applying judicious combination of pipelining and parallelism in order to produce turbo decoder architecture with remarkably high throughput.

Jointly optimized equalization and decoding (also known as turbo equalization) has gained considerable interest of the research community to compensate for the channel impairments due to fading and ISI. However, relatively little work has been carried out on implementation of reduced complexity turbo equalizer. Due research emphasis should be laid on designing efficient architecture of a reduced complexity turbo equalizer using soft interference canceller and parallel SISO decoder, which can accomplish high throughput requirements of wireless applications.

The work recorded in this dissertation has therefore concentrated on the design and development of efficient high throughput turbo decoder architecture suitable for high throughput application. By relaxing some of the constraints, the designed architecture can be targeted for hand held devices which are typically operated by battery power and are meant for real time operation. The major directions in which the present work has progressed can be summarized as follows:

- Design and implementation of area efficient architecture for high throughput turbo decoder based on parallel processing of sliding window Log-MAP algorithm.

- Develop high speed SISO decoding module to accomplish high throughput turbo decoder based on pipelined architecture that reduces the critical path delay of the decoding core.
- Conceive a new algorithm and architecture by combining parallel processing and pipelining technique as an efficient means of enhancing the throughput significantly.
- Design and implementation of a collision free interleaver suitable for a highly parallel and pipelined turbo decoder.
- Design and implementation of reduced complexity turbo equalizer based on soft interference cancellation (SIC) method.

1.3 Summary of Contributions

In this dissertation, various issues related to practical implementation of high throughput turbo decoder have been addressed. Major contributions of the research work embodied in the present thesis are given next.

- An area efficient turbo decoder has been designed and implemented based on sliding window Log-MAP algorithm. Trellis level parallelism coupled with high speed add-compare-select-offset-add (ACSO) architecture has been incorporated as an efficient means of realizing a high throughput turbo decoder.
- A high speed soft-in-soft-out (SISO) decoding architecture has been developed. The work considers the sub block interleaved pipeline architecture to process

the entire data frame with the highest operating frequency reported so far. The design is based on four-stage pipelining of the decoding core and a novel normalization technique that has been proposed in this work. The proposed design integrates addition of the correction factor and normalization of the state metric in order to reduce the critical path delay for realizing of high speed decoding module.

- The work has combined the strengths of pipelining and parallelism to considerably enhance the throughput of the decoder that was designed solely on the principle of parallelism. With negligible additional area overhead, turbo decoder architecture based on combination of both pipelining and parallel processing has been implemented.
- Efficient architecture has been designed and developed to accomplish collision free interleaver. The Quadratic Permutation Polynomial (QPP) based crossbar switch provides a dynamic and temporal interconnection between the set of pipelined parallel workers and the interleaver memory. Collision free memory access has been ensured by memory sub banking scheme and a switching schedule appropriate for the pipelined parallel turbo decoder.
- An iterative turbo equalizer based on Soft Interference Canceller (SIC) has been implemented in this work. The proposed architecture for reduced complexity turbo equalizer displays performance which is sufficiently close to that of the complex minimum mean square turbo equalizer.

1.4 Organization of the Dissertation

The present thesis has been organized as follows.

Chapter 1 outlines the objectives and motivation of this work. Summary of the contributions and the thesis organization are also specified in this introductory chapter.

Chapter 2 reviews the basic concepts of digital communication system and important theory on turbo code which have been used extensively throughout this thesis. It also presents a survey on diverse research activities related to the existing algorithms and architectures for high throughput convolutional turbo decoder. Subsequently, the principle of soft interference canceller based turbo equalization has been briefly discussed.

Chapter 3 discusses the architecture and the implementation of highly parallel turbo decoder for throughput improvement. The synthesis results for the proposed architecture have also been included.

Chapter 4 is dedicated to the concept of applying a combination of pipelining and parallel processing with a novel normalization technique to enhance the throughput of the turbo decoder further. The key results from the hardware implementation of the proposed architecture are given as well.

Chapter 5 discusses about the need of collision free interleaver architecture for parallel turbo decoder and describes an efficient implementation of the collision free interleaver. The collision free interleaver architecture has been further optimized for the combined pipelined parallel turbo decoder.

Chapter 6 focuses on implementation details of the architecture for reduced complexity turbo equalizer based on soft interference canceller (SIC).

Chapter 7 finally summarizes the overall achievement of the present research work recorded in the thesis, and identifies some future research directions in the relevant fields.