

Abstract

Turbo code has received considerable attention as a novel class of forward error control codes since its introduction in 1993. Because of its exceptional performance closely approaching the channel capacity limit prescribed by Shannon, various communication standards such as 3GPP-LTE, IEEE 802.16d and IEEE 802.16e have already adopted turbo code as their channel coding scheme. The outstanding performance of turbo code is however achieved through large latency of the iterative decoding algorithm, which poses significant hurdle in the way of its high-throughput applications. The present work has therefore focused on design and development of efficient parallel implementation for a high-throughput turbo decoder. The design of the component decoder has been optimized so as to achieve low power implementation. Performance enhancing techniques such as parallel processing and pipelining have been applied to achieve further enhancement in throughput. A novel normalization technique that eliminates the need of a full adder stage from the state metric calculation unit has been proposed and incorporated in the design of the decoder. A collision free interleaver has also been incorporated in the proposed pipelined parallel turbo decoder to reap high throughput. Combining iterative turbo decoding with equalization has been an attractive proposition to offset performance loss due to channel imperfections. Turbo equalization based on soft interference cancellation

(SIC) offers tremendous complexity advantage compared to the originally proposed trellis based soft in soft out (SISO) equalizer. The present work has therefore gone on to incorporate a novel architectural strategy to enhance the performance of the SIC based turbo equalizer. The proposed architecture computes the conditional expectation of the transmitted symbols while considering the channel information along with the extrinsic information obtained from the parallel SISO decoder. Architectural analysis shows negligible additional area and power overhead for the decoder parallelism while compared to the traditional non-parallel architecture. Simulation results have demonstrated the improved efficacy of the proposed scheme in mitigating inter-symbol interference (ISI) effects when compared with that of the minimum mean squared error (MMSE) turbo equalizer. The proposed SIC based turbo equalizer therefore fulfills the requirements of high throughput communication to compensate for adverse channel conditions.

Keywords: turbo code, high throughput decoder, pipelined parallel architecture, collision free interleaver, SIC turbo equalizer