Abstract

Assertions are *formal properties* that capture specific functional requirements of a design. In the digital circuit domain, assertions are broadly checked in two ways, namely by monitoring them during simulation, and by formally checking them with model checking tools. The former is more popular in industrial practice, since it has marginal computational overhead and is free from scalability limitations.

With the increased integration of analog and mixed-signal (AMS) components in large scale integrated circuits, studying the extension of assertion specification and monitoring techniques for validating AMS designs has been an interesting new direction for the verification community. This thesis presents some of the initial results and approaches towards studying assertions from a mixed-signal perspective.

The primary contributions of this thesis are as follows:

1. The thesis studies language extensions for capturing AMS design intent from a logical perspective, and studies the tradeoff between complexity and expressibility.

2. The thesis studies the problem of precise evaluation of specified assertions during simulation and analyzes its relation with the choice of time steps and sampling granularity by the simulator.

3. The thesis looks at languages that allow modeling of the design intent using fuzzy propositions and fuzzy timing requirements and presents runtime evaluation technique for such properties.

Additionally the thesis presents the development of a tool flow for assertion monitoring over standard industrial AMS simulators, and empirical evaluation of the proposed techniques using industrial test cases.

It is anticipated that the research presented in this thesis will encourage other researchers to advance the state of the art in this area, and will motivate the industry to adopt some of these methods into industrial verification practices.