Chapter 1

Introduction

1.1 Single Inductor Multiple Output (SIMO) Converters

The proliferation of portable equipment, such as Cell phones, MP3 players, PDAs, Laptops, wireless sensors and automotive applications is promoting extensive research and development in their design. The number of features implemented in such devices is also on the rise leading to multiple supply voltage levels with different load requirements, all of which are powered by a rechargeable source such as Lithium-ion (Li-ion). Nickel Metal Hydride (NiMH) or Silver Zinc battery [1]. Figure 1.1 shows an architectural block diagram of one of today's portable laptops along with its applications. Each of the sub-modules, as illustrated, provides functions, such as LED backlight, liquid crystal display (LCD) monitor, and several signal-processing utilities. Applications may thus require step-down, step-up or at times even a bipolar supply (e.g., in flat panel LED displays) from the same battery. Bipolar supply also finds a wide range of application in Organic Light Emitting Diodes (OLED) [2]. Active-Matrix (AM) panels of OLEDs require a different voltage supply for each color (Red, Green or Blue) to optimize efficiency and quality of the display (viz., brightness, contrast and vividness). Multiple supplies also find their application in internal blocks of many portable devices, such as LCD screen, audio, PLL, motor, DSP, etc [3]. As a result, the design of power management IC typically comprises boost to step-up, buck to step-down, buck-boost to generate negative supply, and linear regulators to meet the different supplies for the high frequency sensitive circuitry.

Conventional implementation of a power management unit (PMU) in today's



Figure 1.1: Block diagram of conventional PMU implementation in today's applications

portable devices (Figure 1.1) comprise several dc-dc converters in parallel to generate non-isolated multiple supplies. Some applications, where isolation is important, employ a transformer that has multiple secondary windings to distribute the energy to those outputs. While the first method requires too many components, including controllers and power devices which increase the system cost, the second does not ensure independent control of the outputs and has a big limitation for the multiple voltage scaling [4–6]. Present day customers are inclined towards more and more miniaturized versions of portable applications and to cater to this requirement, designers are trying to bring the entire converter, even the passives on chip [7]. Further, the longer the battery life, the larger is the market demand for that device. To meet this requirement, efficiency of the converter needs to be maximized by minimizing the losses. To achieve this, switching regulators are preferred. However, for sensitive applications viz,. RF transmitters and high frequency applications, a clean supply is mandatory and consequently linear regulators are chosen over switching regulators. In addition, leakage inductance and cross-coupling amongst the windings cause a serious cross-regulation problem [8, 9]. Thus along with EMI effect it generates large noise and affects system performance. Furthermore, both the methods require 'n' inductors which make the system too bulky and costly with at least '2n' power switches. Hence weight and volume would also cause a packaging problem with increased cost.



Figure 1.2: A single-inductor approach to multiple supply level implementation

The most popular solution of late, among those proposed in the literature, is a single-inductor multiple-output (SIMO) converter based on buck and boost-derived topologies (Figure 1.2) [3, 10–12]. The topology uses a single inductor, acting as a pseudo current source, to generate the multiple outputs. In the process it eliminates many problems of parallel dc-dc converters. Use of SIMO topology brings down the number of components viz., switches and inductors. Hence switching and conduction losses gets reduced simultaneously. To understand its implication on inductor design we can compare the inductor required for a multiple output in SIMO topology to the inductors that are needed for a comparable parallel converter. However the significant

point that may be noted here is that a large inductor may be more efficient than a combination of smaller ones. The coupling losses amongst the inductors (like that in a parallel converter) can be avoided using this topology [13–15]. This approach allows a reduced usage of bulky external components, such as inductors, capacitors and power MOSFETs and it consequently produces a significant saving on overall equipment cost, size and weight, which is strongly desired for this class of applications. The cross-talk effect amongst the output terminals is reduced using a single inductor.

1.2 Survey of SIMO Converters

As explained in the previous section, the SIMO dc-dc switching converter with its advantages can serve as a possible replacement to multiple switching converters. However, this class of converters comes with its associated drawbacks [16, 17]. All the outputs being coupled to the same switching node, all of them suffer from a crossregulation effect when there is a load change in any one or all of the outputs. This tends to destabilize the system performance. An improper design of the dead-band circuit for the switches would lead to shooting up of the switched node voltage and eventual destruction of the power switches [4]. To avoid this cross-regulation problem, a freewheel switch may be connected across the inductor so as to decouple the functionality of the outputs, which in turn reduces the efficiency of the converter [13, 14]. With multiple output nodes coupled to the switching node in this system configuration, the system operation, control and design turn out to be quite complex as compared to the conventional buck and boost switching regulators.

A survey of the available patents on SIMO configuration brings out a diverse set of topologies to generate multiple supply levels [18–32]. However, principally the SIMO class of converters can be categorized into two broad sub-classes, based on the supply level that can be generated at the outputs, viz., buck-derived and boostderived configurations. Only a few publications analyze the operating range, steady state and dynamic performance for this class of converters. Existing literature and products illustrate a wide range of operation and control applied to SIMO converters. In general, the inductor functions as a current source driving the outputs, therefore, it is the manner in which the inductor current is switched, that defines the operation of the converter. The inductor current is switched in two possible manners viz., i) *Time-Multiplexed Switching* and ii) *Current-Shared Switching*. Finally, when it comes to the choice of control scheme the range is very diverse. Some have adopted analog control [33, 34] and some digital (FPGA, DLL etc.) [35, 36]. Amongst analog control techniques incorporated there is a diversification of voltage controlled and current control techniques. While [10, 37, 38] have used freewheel switch across the inductor to decouple the outputs using time-multiplexed switching [30, 35] have stuck to current-shared scheme to operate in CCM. Amongst those that uses freewheel, a couple have tried to feed back the wasted energy in the inductor to the source to make up for the efficiency. In a few, constant switching frequency is incorporated whereas in energy conserved switching is taken up in some. However, what is lacking is an accurate model that can analyze and predict the system performance. A control methodology that can reduce cross-regulation at the outputs while maintaining system stability is still a major concern.

The following sections will illustrate the works on analysis, design and control of SIMO converters available in the literature, patents in this field and market products on SIMO dc-dc converter.

1.2.1 Literature Review

The review of the existing literature can be categorized under three heads viz., i) the available SIMO topologies and their scope of generating outputs, ii) the scheme in which the inductor is switched to deliver the required loads at the outputs in discontinuous conduction mode (DCM), pseudo-continuous conduction mode (PCCM) or continuous conduction mode (CCM) operation, iii) the ways in which these SIMO class of converters are analyzed to predict the system performance and iv) the ways in which the various SIMO structures are controlled. It is understood that all the above mentioned aspects are co-related but still they would be taken up one at a time, addressed and revisited as needed for easier understanding.

1.2.1.1 Existing SIMO Topologies

The most popular solution of late, among those proposed in the literature, addresses SIMO dc-dc converters based on buck and boost-derived topologies [16, 17, 37]. Quite a number of works on SIMO switching converters have been reported over the last decade which are capable of generating buck and/or boost outputs simultaneously [1, 4, 39–41] However very few work present a SIMO architecture that is capable of delivering an inverted output along with positive buck and boost outputs. Some

recent reports in the literature show simultaneous buck and boost output operation. As in case of generation of inverted output from a dc supply, traditionally, buck-boost topology has been used. In SIMO configuration, only a couple of works have been reported which generate negative outputs along with a boost output but the negative output is not independently controlled and the output level is defined by the positive boost output [42, 43]. However, no topology generates independently controlled negative and positive outputs simultaneously in multiple-output configurations with a wide range of the output voltages. Thus a topology capable of delivering multiple-outputs, each with any level of voltage (positive/negative step-up/step-down), using a single-inductor from a single supply will be an ideal desired solution.

1.2.1.2 Inductor Current Switching Schemes

As mentioned, available literature shows two types of inductor current switching scheme viz., time-multiplexed and current-shared, each with its own pros and cons. The two schemes are differentiated by the way the energy stored in the inductor is delivered to the outputs. The time-multiplexed scheme can be said to multiplex some switching converters and consequently the charging and discharging of the inductor for a specific output is distinct and decoupled from the rest. On the contrary, in the current-shared scheme, within one cycle the inductor stores the total energy initially and eventually distributes them amongst the outputs. In this methodology the outputs are coupled amongst themselves. This has been illustrated in details in Section 2.3 but will be briefed on the reviews in this section. Figure 2.4 illustrates the inductor switching in time-multiplexed scheme while Figure 2.4 explains that of the current-shared technique.

• Time-Multiplexed Switching Operation:

In time-multiplexed switching, one switching cycle is broken down into slots and each slot is allocated for a corresponding output where the inductor is charged and subsequently discharged to drive that output. Each such slot can be seen as an energizing cycle, where each energizing cycle drives one output. Thus, the time-multiplexed switching scheme can also be named as *Multiple Energizing Switching Scheme*. The operation is transformed into a multiplexed single-inductor single-output (SISO) operation and in the process the outputs are decoupled (cross-regulation amongst the outputs is reduced). The inductor current has to be freewheeled in between the phases to emulate the DCM in the

CCM.

The time-multiplexed switching scheme has been incorporated in many works of literature. [13, 14, 44] are based on the boost-derived configuration and generate multiple boost outputs while [10] generates buck outputs since it is based on buck-derived configuration. [37] presents buck, boost and inverted outputs together using buck-boost topology. Being based on time-multiplexed switching scheme, all of the above mentioned works function in either DCM [10] or PCCM [14] with quite a large amount of ripple in the inductor current and thus does not support high load operation.

• Current-Shared Switching Operation:

Unlike time-multiplexed scheme, in current-shared switching the inductor is charged only once in the entire switching cycle to an amount so as to discharge and drive all the outputs consequently. Thus, it can be viewed as a *Single Energizing Switching Scheme*. There is no time between each discharging cycle of the inductor to decouple the outputs, consequently cross-regulation effects amongst the outputs arise. Still, this scheme has an edge over time-multiplexed scheme as detailed out in literature. [11, 42, 45] presents SIMO configurations capable of generating buck and boost outputs in current-shared scheme. These operate in CCM and deliver high loads at the outputs.

Although the current-shared method increases cross-regulation effects, it tends to produce smaller output voltage ripples and faster control loops, both of which translate to higher (ac and transient) accuracy. Consequently, this methodology enables operation at higher loads in the outputs. Subsequently, for the same ripple voltage, output capacitors required in the current-shared event are smaller, and the operating switching frequency can be higher (i.e., higher bandwidth). This thesis in its scope will focus on the operation of SIMO converters in current-shared mode so as to harness the associated advantages.

1.2.1.3 Existing Analysis of SIMO Structures

Numerous critical issues are involved in the design of SIMO converters in currentshared switching scheme. As mentioned an accurate model for SIMO class of converters is not reported in literature. Thus predicting the system performance and concluding on a robust control scheme to tackle the challenges is a significant issue.

Nonlinear analysis has been extended to multi-input multi-output dc-dc power electronic circuits, such as multi-cell converters [46, 47] and multi-channel converters [48-50] and the presence of chaotic behaviour in them has been brought out in [51, 52]. Several topologies and strategies for controlling SIMO converters can be found in [38]. Different approaches under CCM operation and digital control with separate regulation of common and differential modes for the output voltages are outlined in [15]. Studying the dynamics of SIMO dc-dc converters is quite complex in terms of the number of energy storage elements, the allowable number of configurations and the operating modes and analyzing the stability of these converters is a real challenge [53, 54]. The existing averaging methods are unable to justify the causes for system instabilities detected in the switched model [55, 56]. A discrete-time model was used in [57] to analyze both the slow-scale (averaged) and the fast-scale (switched) dynamics and could predict a variety of instabilities that can occur in the system. In [58], fast scale instabilities are produced when the stability analysis is carried out because the ripple of the signal is overlooked, whereas those instabilities are associated with the ripple itself. A discrete model is used for high frequency converters. The flip bifurcation in current mode controlled boost converter and elaborated models including statistical analysis are in [59, 60].

In [40, 61], a rigorous analysis of steady-state operation has been conducted to develop useful equations for design purposes. In the "mix-voltage" operation proposed, the input voltage can be lower than one of the output voltages, as opposed to conventional "pure-buck" operation in which input voltage must be higher than both output voltages. In most of the averaged modeling technique used in literature, it can be found that the ripple information of the inductor has been overlooked. Conventional state space averaging technique is not principally based on accumulating the ripple information but on averaging the inductor current over one switching cycle. These overlooked information leads to lack of accuracy in the existing models and system instability since ripple in the inductor current and the switching sequence are the key deciding factor for the output levels.

1.2.2 Control of SIMO Class of Converters

Both buck-derived and boost-derived converters have been operated in time-multiplexed and current-shared switching schemes. Various control methodologies have been adopted to control, stabilize and reduce cross-regulation amongst the outputs of SIMO operated in DCM, PCCM and CCM. This section will review the control techniques presented in the literature. A summary of this section is presented in Table 1.1.

Time-multiplexed switching decouples the outputs and thus eliminates the scope of cross-regulation amongst outputs. However, this operating condition does not allow a CCM operation, so it cannot be operated at high loads. A SIMO with two boost outputs has been presented in [10, 14]. These operate in time-multiplexed switching with voltage mode control. A freewheel switch is used across the inductor to decouple the operating slots.

In [35, 62] the working principle is achieved through counting and comparing the adjacent freewheel switching periods. To ensure PCCM, the controller modifies the duration of each phase, $\Phi 1$ and $\Phi 2$, to equalize the length of each freewheel switching.

A two output SIMO with buck outputs is presented in [63]. The control method is DLL-based that avoids the use of the complex error amplifier and its compensation network. Error amplifiers limit the operating bandwidth, leading to a sluggish closedloop response. The DLL is limited by its acquisition time which is in the order of nanoseconds. DLLs also enable efficient implementations, due to their simplicity. They yield a first-order open-loop transfer function, thereby having more relaxed trade-offs among gain, bandwidth, stability and accuracy. Once the DLL locks onto the voltage regulation error, the duty ratio of the active sub-converter is determined by varying the peak inductor current.

In the two output boost converter presented in [44], when the total time required to complete one set of the energy transfer from the input is longer than one fundamental period T, the switching period extends to 2T, 3T, etc. depending on the total load. The switching frequency is then automatically hopped to $\left(\frac{1}{n}\right)$ (where n=1...5 in this design) times of the switching frequency, where the switching noise spectrum of the system can be predictable. This charge control auto hopping (CCAH) control is very easy to be realized in this sequential-control because no fixed time slot was assigned to each output. During load transient, CCAH control not only need to choose the required switching frequency but also need to ensure to deliver a constant charge to the unchanged outputs by some simple circuits.

Bayer [30, 37] presents a four output buck and inverted output with the control of the individual channels managed by a state machine (outer loop). This controls the power stage switching pattern and allows the hysteretic converter to run in a PCCM to guarantee a high power conversion capability. The second loop works as a variable peak current control to minimize the inductor current. All the above said techniques adopt time-multiplexed switching scheme and thus suffer from the fundamental problem of operating at low load currents. Operating at higher load current requires a current-shared operation that brings in cross-regulation. This thesis is focused at high load operation of SIMO converters and the subsequent paragraphs deal with the existing current shared techniques.

A series of work by Maloberti, presents SIMO converters in buck-derived [11, 64] and boost-derived [8, 65] configurations operating in CCM. The same control methodology has been applied to both the configurations. Several PWM controllers are driven by suitable linear combinations of output errors, which can sustain large load currents, but has large ripples and significant cross-regulation problems. The loop control is a simple diagonal coefficient matrix; the control of the main switch is done by the compensated value of the sum of the errors from the two outputs. One of the output switches is controlled by the compensated difference of errors and the other output switch is the inversion of the prior. The sum of the errors indicates the total power needed by the converter and accordingly the main switch is turned ON to charge the inductor. The method is heuristic in generating the diagonal terms and is not generic for any set of parameters. The reduction of cross-regulation is also not significant enough.

Two output buck implementation with a digital control using an FPGA device is shown in [15, 17, 36]. All the three works are defined by the same control mechanism. The digital control architecture includes a separate regulation of common-mode and differential-mode output voltages. A set of provisions, such as the introduction of an adaptive gain of the differential-mode regulator and a non-linear evaluation of the common-mode voltage, has improved the system dynamic response at different load conditions. Differential mode loop gain is a function of the load current which is very difficult to sense and an accurate realization of the co-efficients is also very difficult to achieve. [68, 69] present an average current mode control in PWM mode for the high side switch only. Current sense is done with zero current detection and current filter circuitry. This works on controlling common mode $(V_{CM} = \frac{V_1 + V_2}{2})$ and differential mode $(V_{DM} = V_1 - V_2)$ voltages. Based on the fact that the ripples and spikes of the two outputs are inverse-phased, a fly capacitor across two outputs has been added to reduce the steady state ripples. [70] is a two output buck, boost configuration with an extension of the same control scheme as the previous works with an extended PWM control. However, not much significant improvement is observed. There are two main control loops in the systems [34, 71]; the common-mode loop which regulates

References	[10]	[14]	[37]	[33]	[11]	[45]	[12]	[34]	[1]	[3]	[17]	[66]	[67]
Process	$0.5 \ \mu m$	$0.5 \ \mu m$	LBC4X Bi-	0.5 μm Bi-	$0.5 \mu m$	Xilinx Spar-	TSMC	TSMC	TSMC	65 nm	FPGA	Stw4141	AN4497
	CMOS	CMOS	CMOS, TI	CMOS	2P5M	tan 3	$0.25 \mu m$	$0.25 \mu m$,	$0.25 \ \mu m$	CMOS			
					CMOS	FPGA	2P5M	1P4M	2P5M				
Topology	Two O/p	Two O/p	Four O/p	Two O/p	Four O/p	Two O/p	Two Buck	Two O/p	Two O/p	Two O/p	Two O/p	Two O/p	
	Boost	Boost	Buck, Boost,	(one boost	Buck	Buck	and Two	Buck	Buck and	Buck	Buck	Buck	
			Inverted	and one			Boost		Boost				
				negative)									
Control	Voltage	Current	State Ma-	MCC with	Voltage	Adaptive	PWM/PFM		PWM/PFM	current	current	PWM,	Voltage
Scheme	mode	mode for	chine with	charge	mode	Current			,	controlled	controlled	PFM	controlled
	control	freewheel	peak current	pump for		Control							PWM
			regulation	negative									
			0	output									
Switching	Time-	Time-	Time-	Current-	Current-	Current-	Current-	Current-	Current-	Current-	Current-		
Scheme	Multiplexed	Multiplexed	Multiplexed	Shared	Shared	Shared	Shared	Shared	Shared	Shared	Shared		
Operating	DCM	PCCM	PCCM	CCM/	CCM	CCM	CCM/	CCM	CCM/				
Condition				DCM			DCM/		DCM/				
						1	PCCM		PCCM				
Input	1.3 V-	1.25 V-	2.5 V to	3.7 V	2.3 V	5 V	1.8 V-2.2 V	2.8 V-5 V	0.9 V-1.6 V	2.7 -3.6 V	2.5 V-5 V	2.7 V -	5 V
-	2.85 V	2.25 V	5.5 V									5.5 V	
Output	3 V, 3.6 V	2.5 V, 3 V	Vmain :	4.6 V to	0.9 V,	3.3 V,	1.25 V,	1.2 V@	0.6 V,	1.8, 1.2,	0.9 - 1.5 V	1.8 V@	15 V@
-			+3.0 V to	6 V, -8 V	0.7 V, 1.1	2.5 V	1.35 V,	400 mA,	1.8 V	1.5, 1		200 mA,	200 mA
			+5.6 V	to -5 V	and 1.6 V		2.0 V,	1.8 V@				1.0 V@	-14 V
			VGH:				2.25 V	200 mA				400 mA	uncontrolle
			+20 V;										
			VGL:										
			-18 V;										
			Auxiliary										
			Output										
			1.8 V to										
			3.3 V										
Frequency	1 MHz	1 MHz	4 MHz			500 kHz	660 kHz	600 kHz	450 kHz	1 MHz	500 kHz	900 kHz	
L	$1 \ \mu H$	$1 \ \mu H$	$10 \ \mu H$	$4.7 \ \mu H$		$4 \mu H$	10 µH	4.7 μH	$10 \ \mu H$		$5 \mu H$	4.7 μH	$15 \ \mu H$
Ci's	$33 \mu F$,	$33 \mu\text{F}, 33 \mu\text{F}$	-	4.7 μ F,		$10 \mu F$,	$33 \ \mu F$ each	$22 \mu\text{F}, 22 \mu\text{F}$	$10 \ \mu F each$	$4.7 \mu\text{F}$ each	$10 \ \mu F each$	$10 \mu F$,	,
	$40 \ \mu F$			$4.7 \ \mu F$		$10 \ \mu F$						10 µF	
Efficiency	88.4 % @	89.4 % @	83 % (max)	82.3 % @	82 %	87 %	80 %	86 % @	80 %			85 %	85 %
	350 mW	320 mW	ì í	330 mW				840 mW,					
								95 %(max)					

Table 1.1: A survey of existing literature and products on SIMO implementations

the total energy by the main loop duty cycle and the differential-mode loop which distributes the energy in the inductor by one of the output duty cycles. Based on the idea of decomposing this cross regulated multi-loop system into several single-loop sub-systems with weak interactions, a novel adaptive common-mode control method is proposed. Here, V_{CM} is adjusted according to the load currents, which can be expressed as $V_{CM} = D_2 * V_1 + (1 - D_2) * V_2$. The weighted coefficient of each channel is proportional to the load current. It is reasonable that the channel which draws more current should have a larger impact on the regulation of inductor current. The results show that the proposed adaptive common-mode control has about 20 dB improvement on the suppression of cross-regulation in low frequency but at higher frequency it persists.

The two output buck converter presented in [45] is a current mode implementation with the outer loops being voltage controlled. The existence of sub-harmonic oscillations has not been dealt with in the work. The control scheme presented in [72, 73] is a current mode control technique. The output, which is more erroneous, is charged for longer time and the other output for a shorter time. The OFF time for the switches is calculated as fractions of the normalized error at the corresponding output to the sum of the total error. Unloading any output, the charging period for the same is skipped for many switching cycles which leads to higher ripples. Thus, definition of the current reference is heuristic and cannot ensure stability.

An ordered power distributive control (OPDC) is presented in [43, 74]. The total power required at the outputs is evaluated and then fed to the outputs based on the priorities demanded. It presents an uncontrolled negative output whose value is dependent on the boost output. The negative output is driven by a diode drop and an output capacitor in charge pump configuration. The rest of the outputs are comparator controlled. In the same series of work, [75, 76] the first three output voltages are controlled using comparators and are called bang-bang outputs, while the last ordered output is P-I controlled with an error amplifier responsible for the converter's total current. Therefore, in this OPDC, all of the errors of the preceding bang-bang outputs are transferred and accumulated to the last output for compensation of the same. However, this output gets worst hit by cross-regulation.

In the next implementation [42], a feedback loop from the output voltage regulates the freewheel period. Since the energy charged in the inductor is more than needed from the output, there is always a freewheeling interval in every switching cycle to monitor this extra energy in the form of current. The average of the sensed freewheeling current is compared with a reference current level, generating an error signal at the output of the compensator. This error signal determines the peak current level of the inductor, similar to a conventional current mode control. The reference current, actually, gives an offset of zero. The output switch is controlled by a comparator with a reference voltage, forming a feedback loop to regulate. This output voltage feedback loop controls the output voltage, but not the total current charged in the inductor. In this manner the inductor, the output capacitor and the equivalent load resistance do not affect the total current loop response.

In [9] a PLL-based multiple-output bang-bang (PMB) control technique is used. The average error of all output voltages is summed with the slope of the ripple-current signal sensed from the inductor, and then applied to the switch control block. The PLL-loop maintains the operating frequency as constant, and the converter can be switched at a higher frequency since adding the current signal can overcome the delay of the voltage loop. An advancement over the previous work forces the remaining inductor current to the supply by switching and comparing through an LC network across the main inductor [77]. When the output load increases abruptly, the main inductor current is insufficient to charge the output capacitors. In this case, the freewheel is not turned on because the outputs have higher switching priority. Then the voltage across the auxiliary output capacitor is reduced by the return current and, consequently, the output of error amplifier increases. Thus, the main inductor current increases to a new value that is sufficient for charging the outputs in one cycle. After the outputs reach their target voltages, the freewheel is turned on again and the control block sets a new steady-state value for the main inductor current.

A Modified comparator control (MCC) [2, 33] uses a two-path pulse width modulation (PWM) channel-control scheme to obtain accurate operation of a PI control on the basis of a speedy comparator control. Unlike conventional PWM switching converters, this PWM channel-control does not control the inductor-charging dutycycle but determines the on-time of the power PMOS switch and the negative output voltage is obtained from an adjustable charge-pump circuit with a PI control. The converter delivers a charge to all outputs at every switching cycle with priority given to the positive output.

A number of work by M H Huang starts off with [16, 78] that employs peak current mode control. A peak current minimum level is set to maintain the steady state level and a peak current dynamic controls the inductor current. The dynamic peak current level is obtained by comparing the voltage reference set from a charge reservation circuit and the compensated feedback from the output voltages. The charge reservation circuit defines the amount of flow of the inductor current in the channels by taking input information from the load currents of both the channels. A nominal improvement of the charge reservation circuit to generate the reference voltages is presented in [1, 12].

The next version in the similar line of work employs average current control method (ACCM) [79]. The inductor current is forced to operate within a range and depending on the level of the inductor current compared to the defined range of the current the outputs are charged. A vector current control method (VCCM) presented in [80] converts the feedback voltage from the output channels to its equivalent current vector. The squares of the current vectors are then added to generate the reference current for the peak current of the inductor current and the time of charging the outputs.

[3] is a SIMO converter for ultra wide band (UWB) applications. Two outputs are driven by an energy conservation mode (ECM). The output voltages are fed back and converted to its equivalent current. The currents are then added and a decision is made for the flow of the inductor current based on the necessity of energy at the outputs. For high load applications, the output voltages are supposed to drop. To make up for this drawback two dc outputs are generated in slave modes and added in parallel to the primary outputs so as to distribute the loads at the outputs. The energy conservation mode is then interleaved between the master and the slave outputs using the ECM controller.

[81] presents a rigorous analysis of steady-state operation and a set of algorithms to operate and control a two output buck configuration. A proposed mix-voltage operation makes the buck derived topology function even when the input voltage is smaller than the output voltages i.e., as a boost output. This gives a new dimension to the operation of SIMO buck-derived topologies.

In conclusion, the essential design challenges of the SIDO converter are low output voltage ripple, reduced cross-regulation and high power conversion efficiency. This work considers an example of a two-output buck-derived SIMO configuration, analyzes and models the system. Finally a control scheme has been developed that can minimize and possibly eliminate the cross-regulation effect in the outputs while maintaining tight regulation and stable dynamic performance.

1.2.3 Product Survey

[82] is a dc-dc converter that supplies all three voltages required by amorphous-silicon (a-Si) and low-temperature poly-silicon (LTPS) TFT-LCD displays. Using a single inductor, it generates independently-regulated positive and negative outputs though the negative output is taken considering the ground as a positive reference. A freerunning variable peak current PWM control scheme time-multiplexes the inductor between outputs (Time multiplexed switching). This control architecture operates at a pseudo-fixed-frequency to provide a fast response to line and load transients while maintaining a relatively constant switching frequency and high efficiency over a wide range of input and output voltages.

[83] once again is a SIMO implementation generating positive and negative outputs for AMOLED displays. The negative output is taken with reference to ground. The configuration uses a combination of PWM and PFM with peak current mode control.

[66] is a single coil dual output synchronous step down DC/DC converter that requires only four standard external components. It operates at a fixed 900 kHz switching frequency in PWM mode. The device can operate in PFM mode to maintain high efficiency over the full range of output currents. The application requires a very small PCB area and offers a very efficient, accurate, space and cost saving solution to fulfill the requirements of digital baseband or multimedia processor supply.

[84] is a voltage-mode, step-up switching converter requiring no expensive currentsense resistors generates the +15 V output using a fixed on time and minimum off time. The negative rail is generated by an external charge pump. Because the negative rail is not regulated, it is not as stable as the positive rail, and varies with current drawn from the positive supply.

1.2.4 Related Patents

Patents filed on SIMO are principally on the topology and the operation these converters so as to generate various supply levels at the outputs. Like the ones quoted in literature and products, the SIMO configuration claimed in the patents can also be categorized based on the time-multiplexed and current-shared switching scheme used in operation. Using the switching schemes some claim to generate only buck, some buck and boost together and some buck, boost and inverted though in most cases the inverted output is generated from one of the positive outputs or by placing the output on the same side as of the input. The next few paragraphs summarizes the innovations made in this field based on the supply levels generated at the outputs and Table 1.2 quotes a few significant ones from the entire list discussed here.

1.2.4.1 Topologies with all Buck Outputs

[23, 85] generate buck outputs using a buck-derived configuration. Whereas the former directly generates buck outputs, the second output in the latter is charged from the first output. [18] claims a triple output buck converter using a single inductor also using a buck-derived architecture. The control scheme for each individual loop is based on the error of that particular output with reference to the sum of all the errors from all the outputs.

1.2.4.2 Topologies with all Boost Outputs

[20] is a boost-derived configuration. It claims high efficiency at light loads/DCM but high load operation in restricted to PCCM. Negative outputs can be generated in buck and boost range by varying the topology and changing the number of switches. Time-multiplexed Mode (TDM) of operation ensures decoupled outputs but with reduced system efficiency. [19, 22] are again boost derived configuration with boost outputs, TDM operation but over multiple cycles. One of the outputs is considered as the primary output, while the other is regulated based on charge scaling. The scaling is based on the required duty cycle of the output. Another boost-derived configuration quoted in [24] has all the outputs as boost. Diodes are incorporated prior to switches to prevent stray currents to flow amongst the outputs when the switches are closed. [19, 29] are examples of time-multiplexed boost-derived topologies configured for boost outputs. In [86] the error signal from the two outputs are compared with same saw tooth ramp as in voltage mode control. The duty cycles achieved is clubbed and provided by a frequency divided clock signal so as to serve the power switches. The control in [73] is based on current mode control and a feed forward control to generate boost outputs. The time at which the input supply has to be turned OFF is estimated and controlled.

1.2.4.3 Topologies with Buck and Boost Outputs

[87] is an example of Buck/Boost operation by selecting the primary switches. The topology of the SIMO and the connections for the switches can be reconfigured to generate various levels of outputs.

1.2.4.4 Topologies with Inverted Outputs

A Boost derived configuration in [25] claims both positive and negative outputs. The inductor current is not bi-directional and the negative output charged from one of the positive outputs is placed on the same side of the supply. [30] records a positive Boost and negative boost output for active matrix LEDs.

Reference	[85]	[88]	[19]	[21]	[31]	[20]	[18]	[87]	[30]
Affiliation	Fairchild,	Seagate,	Intel Corporation,	Sigmatel, AS,	New York, USA	Hong Kong Univ	Freescale Semi-	Nujira Limited,	Ti, GmbH
	South Port-	Shakopee,	Santa Clara, CA(US)	TX			conductor, AS,	Cambridge	
	land, ME(US)	MN(US)					TX		
Filed Date	24^{th} April, 01	15 th July, 04	17 th Aug, 04	20^{th} Dec, 05	25^{th} Sep, 08	7^{th} Oct, 08	26 th March, 09	15^{th} May, 09	15^{th} May, 09
Innovation	Multiple output	Boost derived	Time-multiplexed	Boost derived	Multiple output	A Boost derived	Triple Output	Buck/Boost	Positive Boost and
	buck converter	configuration	switching cycle for	configuration	converter where	configuration,	Buck Converter	operation by	negative boost out-
	with only buck	with both	generating the vari-	with boost	the outputs are	high efficiency at	using a single	selecting the pri-	put for active ma-
	outputs	positive and	ous boost outputs	outputs, TDM	charged based on	light loads/DCM	inductor with	mary switches.	trix LED's. negative
		negative outputs		operation but	distribution of	and higher load	an efficient	Only one output	output is generated
		achievable. The		over multiple	energy. The con-	operation in	control scheme	switch which	by using the negative
		negative out-		cycles. One	verter can have	PCCM. Nega-	running on an	gets connected	connection by mak-
		put is on the		primary output,	different switch-	tive outputs can	algorithm for	to the respec-	ing a common ground
		same side as of		other is regu-	ing patterns	be generated in	the error signal	tive output to	configuration.
		the supply and		lated based on	for different	Buck and Boost	corresponding	generate dif-	
		thus the current		charge scaling.	switching cycles.	range by varying	to a particular	ferent outputs.	
		need not be		The scaling is	OPDC, based on	the topology and	output w.r.t the	Independent	
		bi-directional		based on the	distribution of	changing the	total error	operation just	
				required duty	inductor charge,	no of switches.		by using the	
				cycle of the	does not nec-	TDM mode of		same inductor.	
				output	essarily ensure	operation en-			
					that turn-on and	sures decoupled			
				Ť	duty cycle for a	outputs at re-			
					specific output	duced efficiency			
					voltage will be				
					always constant				

Table 1.2: A summary of innovations in the field of SIMO design

Negative output is generated by making a common ground configuration. [31] is example of another multiple output converter where the outputs are charged based on distribution of energy at the outputs.

[23] presents a configuration which can produce an inverted output but then the output has to be on the same side as the supply. The discharge of inductor current is used to charge the load capacitor placed on the same side of supply.

[20] comes out with another philosophy of generating multiple outputs with one being placed on the same side of the supply. The primary output feeds the secondary output once it's charged from the supply for the first part of the charging cycle. However, the philosophy of simultaneously generating all kinds of output from one topology itself does not hold good. The method of generating buck, boost and inverted outputs from the same topology using the inductor current ripple is not yet claimed.

1.3 Motivation for the Thesis

As discussed earlier, SIMO converters stand out to be a very good alternative to existing parallel converter configuration in PMU's for portable applications. However they come with their associated disadvantages. The operation of this class of converters is primarily defined by the switching sequence of the input and output switches, the ripple in the inductor current and the system parameters viz., value of inductance, amount of loads in the outputs etc. Unlike existing conventional single-output dc-dc converters, the steady state and dynamic system performance of this class of converters cannot be analyzed following the conventional switched average modeling. No accurate methodology exists in the literature to analyze SIMO converters, nor have the operating zone for the same been explored thoroughly. As a result SIMO converters described in the literature, deliver only buck and/or boost outputs. The existing averaging methods assume the ripple in the inductor current to be very small, thus the fundamental information in the operation of SIMO converters is overlooked. Consequently, the instability phenomena detected in the switched model in left unjustified. The coupling among the outputs leads to cross-regulation that drastically affect the system stability and performance both during steady state and transient operation. Optimizing the closed loop performance of these converters, specifically during transient operation, has been a real challenge. The problem of minimizing cross-regulation for independent control of all the outputs and at high load current

has been a serious issue for SIMO converters. The management of dead time between the switches is also an important aspect that needs to be taken into account. A misjudged dead time can either lead to shooting up of the switched node eventually leading to breakdown or burning of the power switches and an overlap can short the coupled outputs. In both the cases the system performance is affected drastically. The dead time factor is a very sensitive factor in the design of SIMO converters and needs to be well addressed.

With the understanding that the operation of SIMO converters is dependent on system parameters, the primary motivation that drives this work is to understand the system accurately so as to develop a control mechanism/schema for the entire class of these converters. The control mechanism should ensure stable system performance under all operating conditions (CCM, DCM and load steps from full load to very light loads), eliminate cross-regulation amongst the outputs which turns out to be a significant issue during load transients, maintain tight load and line regulation. A modeling technique should be developed that can justify the system instabilities and accurately replicate the system dynamics since the conventional averaging technique does not hold good. Without an accurate model it becomes very difficult to predict the system, the dc, ac and cross-regulation parameters. Consequently, developing a control scheme that can minimize such cross-regulation would become very difficult if the system is not analyzed accurately.

1.4 Contribution and Organization of the Thesis

The above section has portrayed an overview of the existing pros and cons of SIMO implementations. The main part of this work is presented in Chapters 2, 3, 4 and 5. Finally, Chapter 6 draws the conclusion from this work and presents a brief description of possible future explorations. Two appendices are provided for further details on the small signal analysis and PCB layout design methodologies.

Chapter 2 proposes an inductor current ripple based modeling approach to model this class of converters. The inductor current is averaged over every operating mode in one switching cycle unlike averaging over the entire period. It has been applied on a two-output boost derived SIMO as an example. The steady state and dynamic performance of the converter obtained through the developed model is validated through simulation and experimentation. The developed model has been used to explore the operating range in various categories of SIMO converters. Subsequently, in Chapter 3, a SIMO topology is discussed that can generate buck, boost and inverted outputs simultaneously. This is the first of its kind when compared to the existing literature. The operating range and system performance as obtained through the analytical model is validated through simulation using ideal components and experimental data. Eventually, a state derivative feedback control methodology has been proposed in Chapter 4. Based on the control methodology, control schemes for SIMO converters are proposed and validated through simulation. The following chapter, Chapter 5 presents the practical implementation of a two output buck-derived SIMO converter in closed loop configuration. It is an experimental validation of the control scheme proposed in Chapter 4. Using the control mechanism, significant reduction of cross-regulation is established experimentally in this chapter.

In Appendix A small signal modeling of a three output boost-derived architecture is carried out using conventional state space averaging to establish that the conventional approach does not hold good for SIMO architectures. The experimental validation of the proposed concepts in Chapter 2, 3, 4 and 5 has been done with discrete components populated on a two layer printed circuit board (PCB), designed in house. The inductor for the power circuit has also been designed in house and mounted on the board. The PCB has been designed such that it can be configured to any amongst one, two or three output buck or boost-derived SIMO configuration. Appendix B discusses important guidelines adopted for designing the PCB. The layout for the same is shown in this appendix.