Abstract

Analog high-level design is rapidly becoming a main topic of interest in an analog design automation process because of its promise to deliver short design closure at much lesser costs. This has motivated us to develop methodologies which make several tasks of the analog high-level design process fast and accurate. This thesis presents optimization-based methodologies for the task of high-level performance model generation, optimal component-level topology generation and high-level specification translation.

This thesis first presents a non-parametric regression-based methodology for the generation of high-level performance models for analog component blocks. The transistor sizes of the circuit-level implementations of the component blocks along with a set of geometry constraints applied over them define the sample space. A Halton sequence generator is used as a sampling algorithm. Performance data are generated by simulating each sampled circuit configuration through SPICE. Least squares support vector machine (LS-SVM) is used as a regression function. Optimal values of the model hyper parameters are determined through a grid search-based technique and a genetic algorithm (GA)-based technique. The generalization ability of the models is estimated through a hold-out method and a k-fold cross validation method. The constructed performance models have been used to implement a GA-based topology sizing process. The advantages of the present methodology are that the constructed models are accurate with respect to real circuit-level simulation results, fast to evaluate and have a good generalization ability. In addition, the model construction time is low and the construction process does not require any detailed knowledge of circuit design. The entire methodology has been demonstrated with a set of experimental results.

This thesis then presents a top-down methodology for the generation of an optimal functional and component-level topology for linear analog systems, starting from a transfer function model of the system. The given transfer functions are converted to state space model which acts as the basis for generation of topologies of the system. The topology exploration process is modeled as a state space

matrix exploration process. Similarity transformation matrix is used as a topology transformation operator. The newly generated topologies have the same behavioral properties, but different performance properties. A simulated annealing-based optimization procedure determines an optimal state space model based on the performances of the models. The optimized state space model is realized by functional component blocks to generate an optimal functional topology, which is subsequently realized by appropriate analog component blocks to generate an optimal component-level topology of the system. As a case study, the thesis presents a methodology for generation of an operational transconductance amplifier (OTA)-capacitor (C) based optimal topology for a 3^{rd} order and a 4^{th} order continuous-time $\Sigma\Delta$ modulator. It is found from the experimental results that the generated topologies are better in performances when compared to that of the commonly used topologies and satisfy the desired dynamic range specifications even under circuit-level non-ideal conditions. The advantage of the methodology is that the designer is able to specify the design goal and the desired specifications of a system at a higher level of abstraction in terms of transfer functions, while the design tool is able to generate an optimal component-level topology of the system directly from the transfer functions in a highly automated manner.

The thesis finally presents a design space exploration procedure for determining the specification parameters of the component blocks of the generated topology such that the desired specifications of the system are satisfied with optimized performances. A meet-in-the-middle approach is followed for constructing the feasible design space. It is constructed as the intersection of an application bounded specification space and a circuit realizable specification space. The former is constructed through a top-down procedure using interval analysis techniques and the latter, via a bottom-up procedure through actual circuit simulations. Least squares support vector machine-based classification principle is used to accurately identify the actual geometry of the feasible design space. Genetic algorithm is used for exploring the feasible design space. The reduced design space speeds up the exploration process. The cost function is computed through behavioral simulation of the entire system and by evaluating the high-level performance models of the component blocks. The final solution point is kept away from the feasible design space boundary, in order to increase the tolerance of the component specifications. The benefit of the methodology is that it is able to obtain practically correct circuit-level specifications of the component blocks of the system through a fast exploration process in a single pass.

The effectiveness of the procedure has been demonstrated by a set of experimental results.

These methodologies form the core of a semi-automated tool for analog high-level design. The methodologies have been implemented under Matlab-Simulink environment. For demonstration of the methodologies, two case studies were chosen: an interface electronics system for MEMS capacitive accelerometer sensor and a continuous-time $\Sigma\Delta$ modulator system. Optimal topologies for these two systems have been generated and specification parameters of the component blocks have been determined using the present methodologies. Finally, they have been implemented at the transistor level based on the derived specifications and are simulated with SPICE. The SPICE simulation results satisfy the desired specifications of the system and match closely with the predicted results. These validate the entire procedure. The entire high-level design process for the interface electronics system is completed in less than ten minutes time and for the $\Sigma\Delta$ modulator system, the design process is completed within an hour. Thus the present methodologies make the high-level design process fast and accurate. In addition, the methodologies can be followed by users with less design experience.