Abstract

Sensor interface electronics has been an emerging area of research which has found its application in diverse fields like biomedical, commercial, navigational, automobiles etc. Real-world signals obtained from sensors have a very low bandwidth and are generally a few hundred microvolts, thereby requiring signal conditioning which, includes amplification and filtering, before being digitized for further processing for information extraction. Thus, sensor application readouts require low sample-rate analog-to-digital converters (ADCs) of medium to higher resolution that consume low power. This research work explores three types of ADCs for sensor readout applications.

The first work presents a 12-bit binary-weighted SAR ADC calibrated using self-subtractive deterministic-dithering to overcome the signal-to-noise ratio (SNR) degradation due to capacitor mismatch. A prototype 12-bit SAR ADC sampling at 8-MHz is realized in UMC 180-nm CMOS process and achieves an effective-number-of-bits (ENOB) of 11.7-bits while consuming 600-μW of power from 1.8-V supply, thereby achieving a figure-of-merit of 22.5-fJ/conv-s and occupying only 0.13-mm^2. The second work presents a transition points-based calibration of SAR ADC using an RC-filtered square wave by looking at the histogram of output digital codes to improve the linearity without any additional analog circuitry. The proposed method is validated with a prototype 8-bit SAR ADC fabricated in UMC 180-nm CMOS process. The SNR of the 8-bit ADC is improved from 42.87-dB to 46.91-dB, and the spurious-free dynamic range (SFDR) is improved from 51.95-dB to 60.61-dB with the proposed calibration method. The next research work proposes a Johnson counter (JC)-based multiphase generation for Voltage-Controlled-Oscillator (VCO)-based ADC for direct digitization of low amplitude sensor signals. A prototype design is implemented at printed-circuit-board level using discrete components achieving a signal-to-noise+distortion ratio ($SNDR$) of 59.2-dB over a 5-kHz bandwidth for 200-$mV_{pp,diff}$ input signal using an 8-phase JC-based VCO-ADC sampled at 2.5-MHz. The proposed design achieves a dynamic range of 64-dB. A variant of SAR-ADC called Noise-Shaping SAR ADC is also explored, a prototype of which is designed in UMC 180-nm to achieve passive first order noise shaping. This architecture achieves an SNDR of 77.9 dB and ENOB of 12.6.

Keywords- SAR ADC, Dithering, Digital Calibration, VCO-based ADC, Sensor interfacing, Noise Shaping, Sensor-to-digital conversion.