ABSTRACT

In bus based Systems-on-Chip (SoC), due to many on-chip communication challenges, the performance, speed, and power consumption of a system can be affected severely. Network-on-Chip (NoC) is an emerging alternative that overcomes this bottleneck for integrating large number of cores on a single SoC. The cores communicate with each other using a router based packet switched network. To determine the performance and cost of NoC, underlying network topology, design of router architecture and link characterization have very crucial roles to play.

This thesis presents a detailed study of Mesh-of-Tree (MoT) topology and explores its promise in communication infrastructure design for 2-D and 3-D NoC. The performance and cost of MoT based 2-D NoC have been evaluated and compared with butterfly fat-tree (BFT) and two variants of mesh network (connecting single/two cores to each router) for 32 cores under same bisection width constraint. Both wormhole and virtual channel routers have been implemented for all the topologies in 2-D NoC perspective. The simulation with self-similar traffic for 2-D NoC places MoT to be the best in terms of performance, for both wormhole and virtual channel router based NoCs. In terms of per packet energy consumption and area overhead, MoT network comes second in the list. Moreover, due to lesser connectivity of the routers, MoT network can be operated at higher frequency compared to others. However, the major bottleneck of any tree based topology in 2-D NoC design is the requirement of longer link with increasing network size. To alleviate this problem, this thesis has extended the MoT topology towards 3-D IC platform. In 3-D implementation, due to the shorter link (about tens of microns) between vertically adjacent layers, the intrinsic problem of having long interconnection wires in tree based topologies like MoT, BFT, fat-tree etc. gets significantly reduced. Simulation results under self-similar traffic show that among different 3-D NoC structures, MoT performs the best at highly localized traffic. For uniformly distributed and low localized traffic, the performance of 3-D MoT is next to the fully connected 3-D mesh network due to its higher bisection width. The average packet energy consumption of 32-core based 3-D MoT is the minimum amongst other networks under consideration. The MoT network has also been evaluated under some real benchmark applications. Simulation results under application specific traffic also show the competitive potential of MoT topology in 2-D and 3-D NoC design. Taking all these observations into account, this thesis establishes MoT to be a strong contender in designing the communication infrastructure of 2-D and 3-D NoC.

KEY WORDS: Network-on-Chip (NoC), Mesh-of-Tree (MoT), Butterfly Fat-Tree (BFT), Globally Asynchronous Locally Synchronous (GALS), 3-D IC, Through-Silicon-Via (TSV).