

Contents

List of Symbols and Abbreviations	vii
1 INTRODUCTION	1
1.1 Introduction	1
1.2 Aim and Motivation	2
1.3 Contributions of the Thesis	3
1.4 Brief Overview of the Thesis	5
1.4.1 Active Termination Scheme for Low-Current Differential Signaling	5
1.4.2 Design and Analysis of Different Current-Mode Receiver Circuit Topologies	5
1.4.3 Design and Analysis of Different Current-Mode Transmitter Circuit Topologies	5
1.4.4 Current-Mode Full-Duplex Chip-to-Chip Data Communication	6
1.4.5 Design and Implementation of Transmitter, Receiver and Hybrid Circuit Topologies	6
1.5 Organization of the Thesis	6
2 LOW CURRENT DIFFERENTIAL SIGNALING	9
2.1 Introduction	9
2.2 Low Current Differential Signaling with Active/Back Termination	10
2.2.1 Current Mode Interface for Low Current Differential Signaling	12
2.3 Complete System Architecture	16
2.4 Conclusions	20
3 CURRENT-MODE RECEIVER CIRCUIT TOPOLOGIES	21
3.1 Introduction	21
3.2 Current-Mode Analog Interface with CCCGTIA	22

3.2.1	Performance of the Design	24
3.3	Current-Mode Analog Interface with CGCSTIA	27
3.3.1	Analysis and Design	27
3.3.2	Post Layout Performance Results	30
3.3.2.1	Measured Results	33
3.3.3	Conclusions	35
3.4	Regulated Cascode Transimpedance Amplifier	36
3.4.1	Analysis and Design	36
3.4.2	Analog Equalizer	39
3.4.3	Post Layout Performance Results	42
3.4.3.1	Measured Results	46
3.4.4	Conclusions	48
3.5	Current Conveyor Transimpedance Amplifier	48
3.5.1	Analysis and Design	48
3.5.2	Post Layout Performance Results	53
3.5.2.1	Measured Results	58
3.5.3	Conclusions	61
3.6	Summary and Conclusions	61
4	TRANSMITTER CIRCUIT TOPOLOGIES	63
4.1	Introduction	63
4.2	Duobinary Transmitter Architecture	65
4.2.1	Duobinary Signaling	65
4.2.2	Duobinary Precoder Architecture	68
4.2.3	Active Terminated Transmitter	68
4.2.4	Post Layout Performance	71
4.2.5	Summary and Conclusions	74
4.3	Double Data Rate Duobinary Precoder Architecture	75
4.3.1	Introduction	75
4.3.2	Double Data Rate Duobinary Transmitter Architecture	78
4.3.3	Dual Mode Duobinary Precoder	80
4.3.3.1	Mode-1	81
4.3.3.2	Mode-2	82
4.3.4	Timing analysis of the precoder architecture	83
4.4	Clock Multiplier Unit	86

4.4.1	Delay Cell with wide locking range	86
4.4.2	Charge Pump With Current Matching	91
4.4.3	High resolution Phase frequency detector	94
4.4.4	Clock generation logic	94
4.4.5	Post Layout Performance	95
4.4.6	Conclusions	100
4.5	Multilevel Polyquaternary Signaling	101
4.5.1	Introduction	101
4.5.2	Polyquaternary Signaling Scheme	103
4.5.3	Fully Differential Current Mode Transmitter Building Blocks .	106
4.5.3.1	Multilevel Precoder	106
4.5.3.2	Polyquaternary Filter	108
4.5.4	Performance of the Design	108
4.5.5	Conclusions	110
4.6	Back Terminated PCIe Transmitter	111
4.6.1	Introduction	111
4.6.2	Active Terminated Current Mode Preemphasis Transmitter .	112
4.6.2.1	Circuit Operation	112
4.6.2.2	Transmitter Output Impedance While Driving	116
4.6.2.3	Active Termination for Incoming Reflections	117
4.6.3	Performance of the Design	118
4.6.3.1	Simulation Setup	118
4.6.3.2	Post Layout Performance Results	119
4.6.4	Conclusions	124
4.7	Current Mode LVDS Output Driver with Back Termination	124
4.7.1	Introduction	124
4.7.2	Proposed Active Terminated LVDS Driver	126
4.7.2.1	Generation of Asymmetric Impedance	126
4.7.2.2	Implementation of Asymmetric Impedance and Circuit Operation	127
4.7.3	Transmitter Output Impedance	130
4.7.3.1	Impedance Offered to Transmitted Signal	130
4.7.3.2	Impedance Offered to Reflected Signals	131
4.7.4	Common Mode Feedback Circuit	133

4.7.5	Low Current Version of Proposed Driver with Active Terminated Receiver	133
4.7.5.1	Low Current Active Terminated Transmitter	134
4.7.5.2	Active Terminated Differential Current Mode Receiver	135
4.7.5.3	Common Mode Matching	136
4.7.6	Performance of the Design	137
4.7.6.1	LVDS Compatible Active Terminated Transmitter . .	138
4.7.6.2	Active Terminated LCDS Transmitter Receiver Pair	139
4.7.7	Conclusions	143
4.8	Back Terminated Current Mode 4-PAM Transmitter	143
4.8.1	Introduction	143
4.8.2	Requirements of Current Mode Transmitter	144
4.8.3	Current Mode 4-PAM Transmitter with Back Termination . .	145
4.8.4	Performance of the 4-PAM Transmitter	147
4.8.5	Conclusions	150
4.9	Summary and Conclusions	151
5	CURRENT-MODE FULL-DUPLEX SIGNALING	153
5.1	Introduction	153
5.2	Current-Mode Hybrid Circuit Topology-I	155
5.2.1	Design and Analysis	155
5.2.1.1	Transconductance Stage	155
5.2.1.2	Design and Analysis of the Transimpedance Stage .	157
5.2.1.3	Complete Current-Mode Hybrid Circuit Topology-I .	159
5.2.2	Performance of the Hybrid Circuit Topology-I	160
5.2.3	Conclusions	164
5.3	Current-Mode Hybrid Circuit Topology-II	164
5.3.1	Design and Analysis	165
5.3.1.1	Design and Analysis of Transconductance Stage . .	165
5.3.1.2	The Transimpedance Stage	167
5.3.1.3	Complete Current-Mode Hybrid Circuit Topology-II	168
5.3.2	Transmitter and Receiver Input/Back Impedance and Transimpedance	169
5.3.3	High Frequency Noise Behaviour	170
5.4	Effect of Residual Echo on the Received Signal	172

5.4.1	Estimation of Received Eye Diagram Jitter	172
5.4.2	Performance of the Hybrid Circuit Topology-II	174
5.4.2.1	Measured Results	181
5.4.3	Summary	184
5.5	Conclusions	184
6	CONCLUSIONS AND FUTURE SCOPE	185
6.1	Conclusions	185
6.2	Future Scope	187
REFERENCES		189
Appendix. A		201
A.1	Transimpedance and Bandwidth of the CG stage of the CG-CS-TIA .	201
A.2	Noise Analysis of CG stage of the CG-CS-TIA	202
A.3	Input Impedance, Transimpedance and Bandwidth of the RGC Stage	203
A.4	High Frequency Noise Analysis of the RGC Front-end	206
A.5	Input Impedance, Transimpedance and Bandwidth of Current-Conveyor Stage of the CCTIA	208
A.6	Noise Analysis of Current-Conveyor Stage of the CCTIA	209
Appendix. B		211
B.1	Input Impedance, Transimpedance and Bandwidth of the Hybrid Circuit Topology-1	211
B.2	Input-Referred Noise Current of the Hybrid Circuit Topology-1 . .	212
Appendix. C		215
C.1	Input Impedance, Transimpedance and Bandwidth of the Hybrid Circuit Topology-II	215
C.2	Output-Referred Noise Current of the Current-Mode Transmitter of Hybrid-II	216
C.3	Input-Referred Noise Current of the Current-Mode Receiver of Hybrid-II	218
CURRICULAM VITAE		221
AUTHOR'S PUBLICATIONS		223