Chapter 1

INTRODUCTION

1.1 Introduction

Aggressive CMOS technology scaling has enabled explosive growth in the integrated circuits industry with cheaper and higher performance chips. In addition, advances in central processing unit (CPU) architecture like multiple cores per CPU and multi-threads per core, as well as improvements in silicon process speeds, have pushed CPU performance to billions of instructions per second[1]. However, CPU speed is of little significance, if limitations in the physical media for chip-to-chip[2], processor-to-memory interfaces[3][4], board-to-board, server-to-server, serial-network interfaces such as FireWire[5], Ethernet[6], and SONET/FibreChannel[7] and local-area network (LAN)-to-LAN connections keep the total processor-to-network[8] throughput low[1].

This limitation has motivated research in the area of high-speed links that interconnect chips and has enabled a significant increase in achievable communication bandwidths. High-speed serial signaling is also growing rapidly in the chip-to-chip interconnection domain, where designers of high-throughput chips are restricted by the limited number of package pins and printed circuit board (PCB) traces. International Technology Roadmap for Semiconductors (ITRS) expects that the aggregate bandwidth of 10-Tb/s with 1000-pins will be required for in multiprocessors by 2010[9]. Enabling higher I/O speed and more I/O channels further improves the bandwidth[10], but these approaches also increase power consumption that eats into the overall power budget of the system. In addition, complexity and silicon area become major design constraints when trying to integrate hundreds of links on a single chip. Therefore, there is a need for building high performance I/O interfaces with

low power consumption and low design complexity.

1.2 Aim and Motivation

High-speed I/O design attracted significant amount of research interest in the last decade[11][12]. Most of the research focus has been on developing high-speed transmitter and receiver circuits[13][14][15][16] that address the non-idealities of the transmission media. These non-idealities include limited bandwidth of the media, adjacent channel interference, different thermal and channel noise sources[17] and reflections that limit the data rates possible. On one hand, there has been considerable effort in utilizing the bandwidth efficiently by using multilevel signaling techniques such as 4-PAM[18], 8-PAM[19] and duobinary[20][21]. On the other hand, there were efforts in enhancing the I/O bandwidth with channel equalization techniques such as linear equalization[22][23], pre-emphasis/deemphasis[24][25], decision-feedback equalization[26]. Recently, crosstalk cancellation techniques[27][28] are introduced to address the issue of adjacent channel interference. There are also efforts in the direction of jitter equalization[29].

To further increase the data rate per pin and efficiently utilize the limited number of channels, full-duplex signaling[10][30] has been explored. The effective pin and wire density of a signaling system can be doubled by using full-duplex signaling to send bits simultaneously[31] in both directions over a single transmission line. High-speed full-duplex communication can be applied to various types of interconnections such as chip-to-chip, processor-to-memory, processor-to-processor and high bandwidth networks such as ATM interfaces, LAN's, satellites and optical networks.

Research in full-duplex communication link design received significant attention in the last decade[31][32]. Single-ended and simultaneous bidirectional link has been reported in[33]. It describes different additional noise sources of a single-ended full-duplex communication link compared to a unidirectional communication link. This single-ended voltage-mode communication link is limited by different voltage noise sources, jitter and difficulties of reference generation at the receiver. To address some of these issues, fully-differential voltage-mode full-duplex communication has been reported in[32]. Mixed-mode full-duplex communication is proposed in[34][35]. These links use a mixed-mode hybrid circuit topology, consisting of a current-mode transmitter and a voltage-mode receiver requiring terminators on both sides. These

passive terminators increase the power consumption for a target signal swing. These links have serious limitations for generating the reference for the slicers. Also, they does a poor job of isolating signals from power supply noise, attenuating signal-return crosstalk and a return ground loop.

All these approaches aim at a common goal of increasing the per pin data rate by utilizing existing low-cost FR4 PCB traces and low-cost analog circuits. However, there is little effort in efficient addressing the reflection related intersymbol interference caused by impedance discontinuities. To address this issue, reported I/O interface circuits use either on-chip or off-chip passive terminators at both ends of the transmission medium. Using passive terminators or dedicated active devices in triode region[36][37] is straight forward solution but inefficient. Since, these terminators not only consume significant amount of power but also generate thermal noise. Things are even worse for full-duplex high speed communication, where it is required to use terminators on both end of the line. Also, these terminators are the return impedances linking the transmitter with its own receiver leading to generation of residual echo. The power consumption per pin, per gigabit of data transmission is a serious issue when the links aim for higher data transfer rates as predicted by ITRS[9]. Therefore, there is a need for developing power-efficient high-speed interface circuits to meet the future data transfer needs.

For an optical chip-to-chip interconnect, it is well known that the input parasitic components deteriorate the bandwidth and noise performance of the pre-amplifier[38]. Usually the front-end of an optical receiver is a transimpedance amplifier (TIA). The design of these TIAs entails many trade-offs between noise, bandwidth, gain, supply voltage and power dissipation, presenting difficult challenges in CMOS technology. The main limitation comes from the large photodiode capacitance. Therefore, novel circuit techniques are required to relax the input parasitic effects. There are efforts to mitigate this photo diode capacitance by using common-gate[39] and regulated cascode[40] TIAs which offer low-input impedance. However, still there is a great need for reducing the input impedance and also input-referred noise current to a low value, to mitigates the speed bottleneck created by the photodiode.

1.3 Contributions of the Thesis

This research work proposes current-mode transmitter and receiver circuit topologies supporting different low-current differential signaling (LCDS) schemes such as, non-return to zero, multilevel and partial response signalings.

One of the main advantages of using the proposed current-mode interface circuits is that, they incorporate back termination at the near-end and active termination at the far-end of the link leading to complete elimination of passive terminator. The second advantage is, the proposed current-mode receivers have low input referred noise than that of a conventional voltage mode receiver and hence improves the signal sensitivity. With the improved sensitivity of the receiver, now the link can operate at a low transmitted current level.

In addition, the proposed receiver topologies have descent dynamic range. This supports different multilevel signaling schemes. Different duobinary and polyquaternary transmitter architectures are explored.

New half-rate duobinary precoder architectures are introduced to implement high speed duobinary precoding. It is important to note that, due to low input impedance, each one of the proposed current-mode receiver topologies is not only suitable for self-termination of a wired link (transmission line) but also they can be used as TIA's for optical links. Input impedance of one of the receiver topologies can be easily tuned to a very low value making it suitable for both high speed optical and electrical links.

To further increase the throughput of the existing serial links, a current-mode full-duplex (CMFD) signaling scheme has been introduced which is supported by two proposed hybrid circuit topologies with current-mode echo cancellation.

Apart from exploring a low-current signaling link, the active and back termination techniques have been applied to existing signaling standards such as, low-voltage differential signaling (LVDS) and peripheral component interconnect express (PCIe), for reducing the overall power consumption.

All of the proposed circuit topologies have been analyzed including their noise and sensitivity performance. For validation of these topologies and the signaling scheme a test chip has been designed in 1.8 V, 0.18 μm digital CMOS technology. The test chip contains a delay-locked loop (DLL) based serializer for high speed serial data generation. To supplement the reported results extensive process corner and Monte Carlo simulations are performed. The performance shows that, the proposed techniques have the potential to upgrade the existing backplane systems with power

efficient interfacing modules for higher bandwidth.

1.4 Brief Overview of the Thesis

1.4.1 Active Termination Scheme for Low-Current Differential Signaling

This work proposes new termination scheme called active/self/back termination, where the termination is integral part of the I/O interface circuits. The port impedance of the I/O interface circuits are made equal to the characteristic impedance of the line. This eliminates the need for separate passive termination resistors of either off-chip/on-chip or dedicated active devices operating in triode region. The proposed termination scheme facilitates low-current differential signaling, a current-mode signaling scheme ultimately leading to low-power I/O interface circuits. The I/O interface circuits designed with this scheme include different transmitters, receivers for half-duplex signaling and hybrid circuit topologies for full-duplex data communication.

1.4.2 Design and Analysis of Different Current-Mode Receiver Circuit Topologies

This thesis proposes new-current mode receivers circuit topologies with low-power consumption, which are suitable for both electrical and optical chip-to-chip interconnect. These receivers input port impedance can be made equal to 50 Ω for matching the characteristic impedance of the electrical interconnect or it can be made very low, even lesser than 50 Ω, as required in an optical interconnect for mitigating the bandwidth determining photo diode capacitance. Detailed design and analysis of these current-mode receivers, namely, cross-coupled common-gate TIA (CCCGTIA), common-gate TIA (CGTIA), regulated gate cascode TIA (RGCTIA) and current-conveyor TIA (CCTIA) are presented.

1.4.3 Design and Analysis of Different Current-Mode Transmitter Circuit Topologies

A current-mode transmitter should provide high output impedance for outbound or transmitted signal and 50 Ω matched termination for reflections. This dual conflicting requirement is met with the new active/back terminated current-mode transmitter topologies proposed in this thesis. The proposed transmitter circuit topologies output port impedance is high for driving signal and the same port impedance is tuned to 50 Ω for reflections. The proposed back termination technique is applied in the design of NRZ, 4-PAM, LVDS and PCIe transmitters. Also, an active terminated high bandwidth duobinary transmitter is presented. New duobinary precoder architectures are presented to address the speed limitation offered by one unit interval delay data feedback loop. The test chip also houses a delay locked loop (DLL) based serializer with an integrated half-clock rate precoder.

1.4.4 Current-Mode Full-Duplex Chip-to-Chip Data Communication

This work proposes current-mode full-duplex chip-to-chip data communication. The advantage of this scheme is presented in comparison with voltage-mode and mixed-mode full-duplex communication and the way to eliminate the terminators on both ends of the line are presented. This work also proposes two new hybrid circuit topologies for current-mode echo cancellation. Complete design, analysis of the hybrid circuits and echo induced jitter analysis are presented.

1.4.5 Design and Implementation of Transmitter, Receiver and Hybrid Circuit Topologies

All the different types of receivers, hybrid circuits and transmitter circuit topologies including precoder, serializer and DLL are designed, fabricated and tested. The design and layout is carried out in 1.8 V, 0.18 μm digital CMOS technology. Successful DC and functionality tests are carried out with the limited test facility available. To supplement the reported results extensive process corner and Monte Carlo simulations are performed and reported.

1.5 Organization of the Thesis

The thesis is organized as follows.

- **Chapter 1:** This is an introduction chapter describing the motivation behind the work, literature survey, background, objectives and highlighting contributions of the present work.
- **Chapter 2:** In this chapter, requirements of current-mode analog interface circuits is discussed and active termination enabled low-current differential(LCDS) signaling is presented. Also, complete system architecture is described.
- **Chapter 3:** In this chapter, design, analysis and performance of new current-mode receiver circuit topologies for electrical and optical link are presented.
- **Chapter 4:** In this chapter, design, analysis and performance of different active/back terminated transmitter circuit topologies are presented.
- **Chapter 5:** In this chapter, current-mode full-duplex communication and its advantages are presented. Also, Design, analysis, implementation and jitter modeling of new current-mode hybrid circuits are presented.
- **Chapter 6:** In this chapter, conclusions to the thesis as well as future directions of this work are presented.