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AUTHOR'S PUBLICATIONS

- [1] Vijaya Sankara Rao P. and Pradip Mandal, "Current-Mode Analogue Interface for High-Speed Low-Current Differential Signalling," *International Journal of Electronics, Taylor and Francis*, vol. 97(9), pp. 1007–1020, Sep. 2010.
- [2] Vijaya Sankara Rao P. and Pradip Mandal, "A new current-mode receiver for high-speed electrical/optical link," *International Journal of Electronics and Communication*, Elsevier, vol. 65(2), pp. 107–116, Feb. 2011.
- [3] Vijaya Sankara Rao P. and Pradip Mandal, "Active Terminated Transmitter and Receiver Circuits for High-Speed Low-Swing Duobinary Signaling," *International Journal of Circuit Theory and Applications, Wiley*, vol. DOI: 10.1002/cta.730, 2010.
- [4] Vijaya Sankara Rao P., Debashis Banerjee and Pradip Mandal, "Active Terminated Current-Mode Pre-emphasis Transmitter for PCI Express Standard," *International Journal of Electronics and Communication, Elsevier*, vol. 10.1016/j.aeue.2010.09.007, 2010.
- [5] Pradip Mandal, Sailesh Pati, Vijaya Sankara Rao P.,, "Active Terminated Differential Current-Mode Receiver for High-Speed Data Communication," in *IEEE NEWCAS-TAISA09*, Toulouse, France, June 28-July 01 2009, pp. 1–4.
- [6] Vijaya Sankara Rao P., Pradip Mandal and Sunil Sachdev, "High-Speed Low-Current Duobinary Signaling Over Active Terminated Chip-to-Chip Interconnect," in *IEEE Annual Symposium on VLSI*, Tampa, Florida, USA, May 13-15 2009, pp. 73–78.
- [7] Vijaya Sankara Rao P., Pradip Mandal, "Self-Termination Scheme for High-Speed Chip-to-Chip Data Communication," in *IEEE International Symposium*

- on Signals, Circuits and Systems(ISSCS),, Iasi, Romania, July 9-10 2009, pp. 1–4.
- [8] Vijaya Sankara Rao, Mrigank Sharad and Pradip Mandal,, "High-Speed Transmitter for Fully Differential Current-Mode Polyquaternary Signaling Scheme," in *IEEE International Midwest Symposium on Circuits and Systems(MWSCAS 2009)*, Cancun, Mexico,, August 2-5 2009, pp. 74–77.
- [9] Vijaya Sankara Rao P., Pradip Mandal, "Current-Mode Echo Cancellation for Full-Duplex Chip-to-Chip Data Communication," in *IEEE Asia Pacific Conference on Circuits and Systems*, Kuala Lumpur, Malaysia, 6-9, December 2010.
- [10] Vijaya Sankara Rao P. and Pradip Mandal, "A New Power Efficient Current-Mode 4-PAM Transmitter Interface for Off-Chip Interconnect," in *IEEE Asia Pacific Conference on Circuits and Systems*, Kuala Lumpur, Malaysia, 6-9, December 2010.
- [11] Mriagnak Sharad, Vijaya Sankara Rao P. and Pradip Mandal, "1.A New Double Data Rate (DDR) Dual-Mode Duobinary Transmitter Architecture," in 24th IEEE International Conference on VLSI Design 2011, Chennai, India, January, 2-7 2011.
- [12] Vijaya Sankara Rao P., Nachiket Desai and Pradip Mandal, "A Low Power 5 Gb/s Current-Mode LVDS Output Driver with Active Termination," *Circuits, Systems and Signal Processing, Springer*, vol. doi:10.1007/s00034-011-9280-2, pp. 1–19, March 2011.
- [13] Vijaya Sankara Rao P., Pradip Mandal, "Current-Mode Full-Duplex(CMFD) Signaling for High-Speed Chip-to-Chip Interconnect," *Elsevier: Microelectronics Journal*, vol. 42(7), p. doi:10.1016/j.mejo.2011.04.007, July 2011.
- [14] Mrigank Sharad, Vijaya Sankara Rao P. and Pradip Mandal, "Half-Rate Duobinary Transmitter Architecture for Chip-to-Chip Interconnect Applications," *Springer: Analog Integrated Circuits and Signal Processing*, vol. doi:10.1007/s10470-011-9621-x, April 2011.