Abstract

Aggressive CMOS technology scaling has enabled explosive growth in the integrated circuits industry with cheaper and higher performance chips. This performance improvement can be fully capitalized as well by increasing the speed of off-chip link. Enhancing the speed of chip-to-chip link, processor-to-memory interface, board-to-board interface, server-to-server, serial-network interfaces make the net processor-to-network throughput improved. This requirement has motivated this research in the direction of high speed serial links. This thesis proposes current-mode transmitter and receiver circuit topologies suitable for low-current differential signaling. One of the main advantages of using the proposed current-mode interface circuits is that they incorporate back termination at the near-end and active termination at the far-end of the link leading to complete elimination of passive terminators. The second advantage is that the proposed current-mode receivers have low input referred noise than that of a conventional voltage mode receiver and hence, improve the signal sensitivity. With the improved sensitivity of the receiver, now the link can operates at low current level. Input impedance of one of the proposed receiver topology can be easily tuned to a very low value making it suitable for both high speed optical and electrical links. New duobinary precoder architectures are introduced to implement high-speed duobinary precoding. To further increase the throughput of the existing serial links, a current-mode full-duplex signaling scheme has been introduced which is supported by two proposed hybrid circuit topologies with current-mode echo cancellation. The active and back termination techniques have been applied to existing signaling standards such as, low-voltage differential signaling and peripheral component interconnect express, for reducing the overall power consumption. Design, analysis and fabrication of a test chip containing all of the proposed circuit topologies have been carried out in 1.8 V, 0.18 μm digital CMOS technology. The test chip also contains a delay-locked loop based serializer for high speed serial data generation. The performance shows that, the proposed techniques have the potential to upgrade the existing backplane systems with power efficient interfacing modules for higher bandwidth.

Keywords: Serial Links, Current-Mode Circuits, Active Termination, Full-duplex