Abstract

Moore's law has been the driver in semiconductor technology, describing the advancement of technological capability since its introduction in 1965. Progress in the field of the nano-scale device resulted in billions of transistors inside a modern-day VLSI chip with almost no room for further miniaturization leading to an eventual slowing down of Moore's law. The slowing down of Moore's law is not just hype but a reality that requires serious attention. More and more transistors are squeezed inside a chip, and consequently, there is not much room left at the bottom anymore. Moreover, the problem of memory-bottleneck in the traditional von-Neumann architecture urges researchers to find an alternative architecture that rectifies this problem. DRAM, SRAM, and Flash are traditional memory technologies rapidly reaching their size and power consumption limits. In addition, due to its restricted endurance, the Flash memory cannot be scaled beyond the current regime. All of these contribute to the quest for emerging technologies that can solve the above problem.

Memristors, an emerging device, also classifiable as Resistive RAM (RRAM), has the potential to answer these problems. A memristor is a two-terminal passive device capable of remembering the charge that previously flowed through it. Memristor, a concatenation of memory and resistor, was known to be fabricated successfully only in 2008 by HP Labs. Memristors exhibit unique properties that support various logic and memory operations, and due to the advancement in memristor-based research, they are expected to be a replacement for flash memory devices in the near future. The unique properties of memristor lay the foundation for an architecture beyond the traditional von-Neumann architecture, commonly known as an in-memory computing architecture (IMC). In IMC, both processing and storage of data can be performed in the same memory unit without the need to have a separate processor and memory. Memristors can be efficiently fabricated as a crossbar array. Diverse memristor-based logic designs have been reported, such as MAGIC, IMPLY-based, BDD-based, AIG-based, and MIG-based, which can be carried out on the crossbar. The lack of mitigation for the sneak-path issue in the memory array is a typical flaw in these systems, resulting in erroneous data processing.

This thesis concentrates mainly on various solutions to the sneak-path prob-

lem and the necessary logic synthesis techniques for in-memory computing on 2D and 3D crossbar arrays. Various operation mapping techniques for these synthesis methods are also proposed to achieve scalable and efficient processing of data. The adopted solutions to fix the sneak-path issue are based on a transistor gating based on the 1T1R cell structure and the use of complementary memristor cells in the crossbar. We also explore the possibility of logic operations on data stored in the crossbar using the MAGIC NOR and Majority gate operations. Experimental results on various benchmark functions show the proposed works' efficiency compared to existing logic synthesis techniques.

Keywords: Memristor; RRAM; In-memory computing; Sneak path; 1T1R; Complementary memristor; Complementary resistive switches; Crossbar; MAGIC.