AUTHOR'S RESUME

Email : baijayanta_ray@yahoo.com , baijayanta@gssst.iitkgp.ernet.in

Address : Flat No: E-220, Sterling Brookside, Kundalahalli Colony

ITPL Main Road, Bangalore – 560067, Karnataka

EDUCATION

Jan., 2007 – April 2010 PhD. , IIT, Kharagpur (Thesis submitted)
July., 2002 – Oct 2004 MS. , Indian Institute of Technology, Kharagpur
July., 1998 – June 2002 BTech(Hons.) , IIT, Kharagpur

SUMMARY OF PROFESSIONAL EXPERIENCE

2007–2011 **National Instruments, Bangalore**
Senior Staff Engineer

2004 – 2007 , 2011- **Synopsys, Bangalore**
Senior R&D Engineer

AWARD

- **B.R.Nag, Design Contest Award for Best Design Entry, 18th Intl. Conference on VLSI Design , 2005**

PATENT

- **Digital Architecture for DFT/IDFT Hardware (US Patent Application Number 20080281894)**