Abstract

Binary Decision Diagrams (BDDs) play an important role in the synthesis, verification, and testing of VLSI circuits and other applications like security, shape analysis of geometric objects etc.

In this work, we have reported a new BDD-based approach for the synthesis of dual-rail adiabatic MUX circuits, which works much better in low frequency application. For high frequency application the best dual-rail logic for BDD-based synthesis is Dynamic Cascode Voltage Switch with Pass Gate (DCVSPG) logic, which we have used as library cell and made logic synthesis more optimized in area and power. As technology mapping has become significant in reducing chip area in terms of number of logical block we have also introduced an efficient mapping algorithm which can map single-rail logic cells like LEAP (Lean Integration with Pass-Transistors) cells from BDD for better optimization in terms of area, power and delay.

Testing of such VLSI circuits is another challenge for chip manufacturer. ATPG (Automatic Test Pattern Generator) is ruling this sector for many years. But circuit realized from special type of graph like BDD an alternative to ATPG can be employed to find test vectors for optimum fault coverage. In this work, we consider the open problem of generating in polynomial time, the exact minimum set of test vectors for detecting all single stuck-at faults in such a BDD-based circuit synthesized with multiplexers. This procedure not only generates the optimal test set in polynomial time, but also obviates the need of employing an ATPG and a fault simulator. We have also reported a simple algorithm for determining the maximum independent set of edges of a BDD that has got direct relation for finding optimal stuck-at-fault test set in a BDD-based circuit.

We have also considered how to detect stuck-at faults when circuit is ON. For this we have reported a BDD-based methodology for designing low power and low area on-line testing (OLT) device which can efficiently detect all the stuck-at faults in smaller cycle time.

Next, in this work, we have designed a BDD-based asynchronous adder that obviates the need of complex ASIC flow. Also, the design takes much less area and power compared to the design with other standard library cell. We have also shown that a slight modification of such circuit can be made secure from external attack like side channel attack (SCA). For both the designs we have achieved a significant amount of reduction in area and power compared to the contemporary designs. We have successfully taped out these chips using TSMC fabrication unit.

Another application of BDD on security has been proposed in the area of internet firewall design. We have implemented a BDD-based packet filter firewall which is robust and more efficient than the existing list-based packet filter firewall system.

Keywords: Binary Decision Diagram (BDD), Low Power Synthesis, VLSI Testing, On-line Testing (OLT), Asynchronous Design, Side Channel Attack (SCA), Firewall.