Abstract

The dissertation presents the subthreshold model of multi gate (MG) junctionless (JL) FETs with scaled equivalent oxide thickness (EOT). In the work, classical physics based models of asymmetric double gate and asymmetric gate all around structures are proposed. The asymmetric double gate (DG) junctionless (JL) FETs includes non-uniform doping arisen due to ion-implantation method. For the same, the models available in literature, to include analytic approximation of non-analytic Gaussian shape, have been studied. It is found that the existing models impart high complexity in the subthreshold solution; henceforth, a simpler linear approximation is proposed for the scaled devices to approximate the piece of the Gaussian curve falling within channel thickness of nano-meter dimension. The proposed approximation is numerically studied to explore the accuracy factor, and subsequently included in the model of double gate JLFETs. Henceforth, with a minimum complexity involved the subthreshold solution of DG JL FETs having structural and doping asymmetries is presented. Further, the literature of subthreshold modeling of JL FETs is explored with respect to implementation of high-*k* gate dielectric and sub-1nm equivalent oxide thickness (EOT). The study suggests the lack of suitable subthreshold model for scaled EOT. Thereby with an appropriate modification in evanescent mode solution, the subthreshold model of asymmetric DG JL FETs is presented which can effectively models the device with sub-1nm EOT. The proposed model is numerically studied for EOT up to 0.5nm using high dielectric constant materials. Further, using the perimeter weighted sum approach the subthreshold model of gate all around (GAA) JL FETs with scaled EOT is developed. For the existing perimeter weighted approach to model channel potential and threshold voltage, a novel subthreshold slope model for GAA JLFETs is developed. Theoretically, the subthreshold model of GAA JLFETs presented can be implemented with all the feasible domain of EOT for devices. However, as per the literature study the EOT of GAA FETs is downscaled up to 0.78nm in the present study. Single layer of Silicon based dielectric, as well as stack of Silicon and non-Silicon based dielectrics, has been considered for scaling of EOT in GAA JLFETs. The corner effect has been incorporated appropriately in the model of GAA JLFETs. The classical model results are numerically studied in comparison to the Sentaurus TCAD tool.

Key words: Subthreshold model, Threshold voltage, Junctionless FETs, Double gate, Gate all around, Asymmetry, High-*k* dielectric, Gate dielectric, Equivalent oxide thickness.