Abstract

In the semiconductor industry, multigate Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are regarded as a potential alternatives to the conventional MOSFETs, especially when the channel length of the device is scaled down below 20 nm. Over the past few years, the multigate MOSFETs have been better choices because of their excellent gate control on the channel and better immunity to short channel effects (SCEs). It is also possible to get enhanced drive current since multiple gates can form multiple current carrying faces in the device's channel. For the design of an IC, it is essential to get an appropriate device model that describes the device's fundamental electrical behavior. In this thesis, a precise analytical modeling framework is presented for the double gate (DG) MOSFET and triple gate (TG) MOSFET. The presented models consider specific physical or operational constraints and the device's intrinsic parameter variations. The models are based on drift-diffusion carrier transport mechanisms. But there are some issues which persist in multigate MOSFET devices. These are e.g., high leakage current, sub-threshold swing limitation of 60 mV/decade, and so on. In this regard, Tunnel FET (TFET) is chosen, which exhibits lower sub-threshold slope, lower leakage current, better immunity to short channel effects, but less drive current (or ON current). Several techniques have been evolved to improve ON current of TFET. This thesis also presents a novel triple metal work function engineered (WFE) TFET, which shows a lower sub-threshold slope and better ON current. Moreover, the analytical models of parasitic capacitances and resistances for TG MOSFET and TFET are developed, providing a detailed understanding of the device's built-in parasitic resistance and capacitance.

All the developed models presented in this thesis are validated against TCAD Sentaurus simulation results to check accuracy. The model results are also verified with the published data to confirm their improvements and novelties. Finally, the

proposed models are invoked in the simulator, based on which a simulation study is performed on triple gate MOSFET and double gate TFET based inverter circuits and their implementation in a ring oscillator circuit.